A Technique to Reduce Cross Talk Between Copper Routes Under a 1 mm Pitch BGA

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Abstract

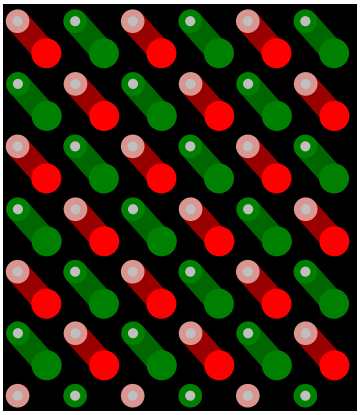
This white paper describes a technique for reducing cross talk between copper routes in 1 mm pitch BGA devices. This method can be used with any integrated circuit device that uses a 1 mm BGA package. The technique is a printed circuit board (PCB) level solution, and is employed at the layout level of a design. This white paper is targeted for:

- Printed circuit board design engineers
- Simulation engineers
- Layout engineers

Introduction

This white paper describes a technique to reduce cross talk between signal routes under a 1 mm pitch BGA, without losing significant PCB real estate for outer breakout routing. The traditional BGA breakout is one BGA pin and one via to allow routing on internal layers. A typical high-speed interface at the BGA breakout using impedance controlled differential pair routing is the standard way of implementing BGA breakout of 1 mm pitch devices. By using the rule of *1 pin 1 via* breakout, as shown in the following figure, and the correct selection of stack-up to allow the correct line width and pitch, it is possible to route multiple high-speed differential pairs from the BGA to any target device or connector. This technique to reduce cross talk uses multiple vias in parallel at the point of breakout. The multiple vias are arranged in such a way as to not disturb the normal routing of signals in the BGA breakout region. This is done by using smaller vias that can be fitted closer together.

Figure 1: **Traditional 1 mm Pitch BGA Breakout Using a One Pin, One Via Solution**



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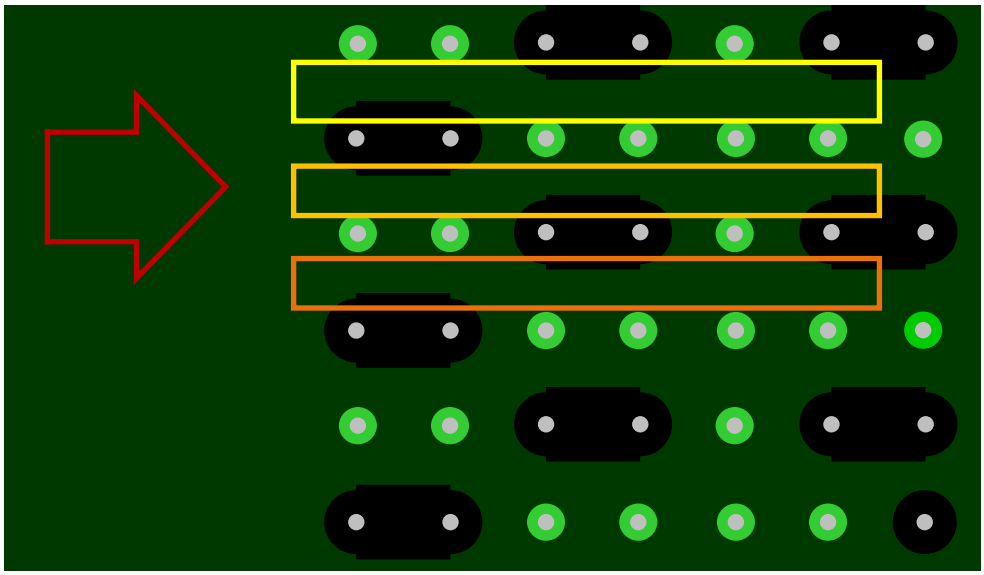
Background on Traditional Techniques

A typical BGA pin is 0.5 mm/19.68th pad, with a 45-degree breakout. The traditional clearance rules to manufacture a PCB include:

- 9 mil drill to trace
- 3 mil trace to trace on internal
- 4 mil trace to trace on outer layers
- 8 mil via drill (finished hole size)

Inside the BGA breakout, exit lanes are created to allow the internal routing of signals from under the BGA region. The typical *1 pin 1 via* 45° breakout creates a structure as shown in the following figure.

Figure 2: **Internal Routing Lanes**



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This *1 pin 1 via* structure is used to create routing lanes on multiple internal layers to allow a clear area for breakout. The following figures show routing on internal layers below the BGA device to break out multiple differential signal pairs.

Figure 3: **Internal Layer 3 (Layer Top — 2)**

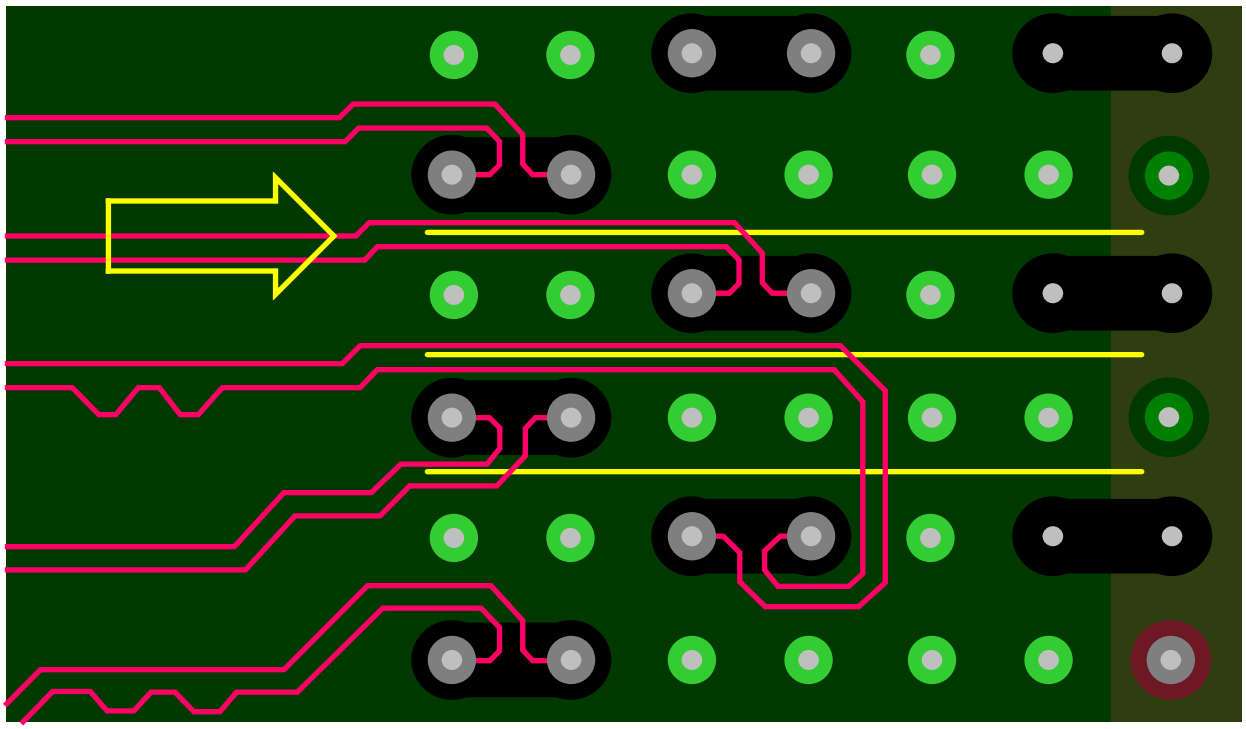

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Figure 4: **Internal Layer 5 (Layer Top — 4)**

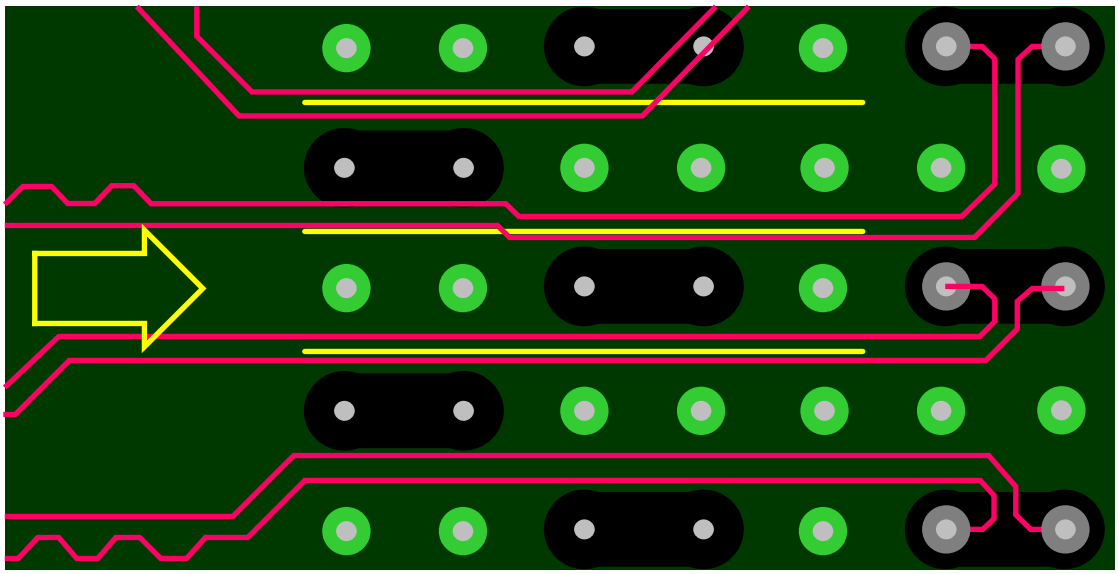

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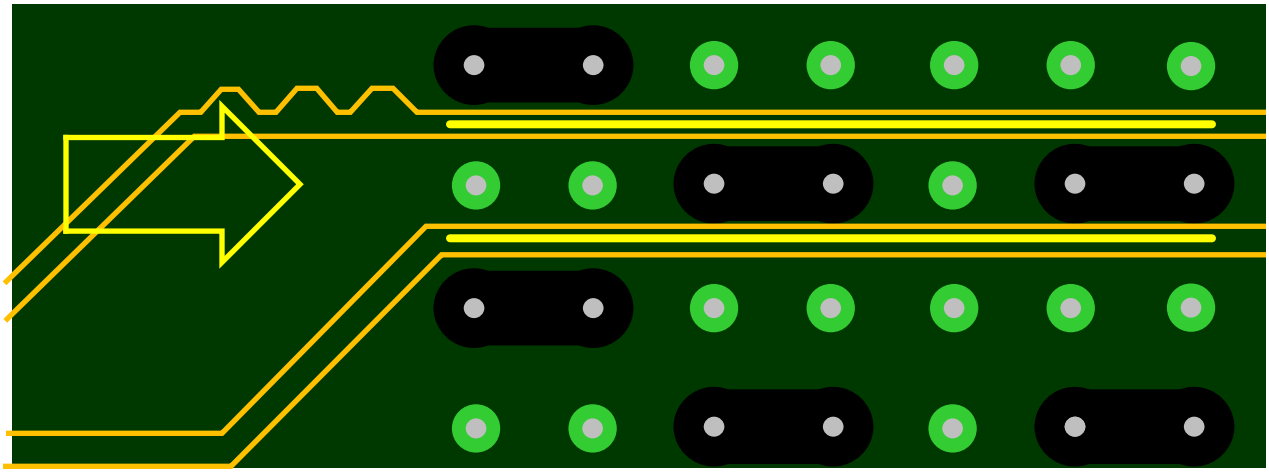
Figure 5: **Internal Multiple Layers of Available Routing**



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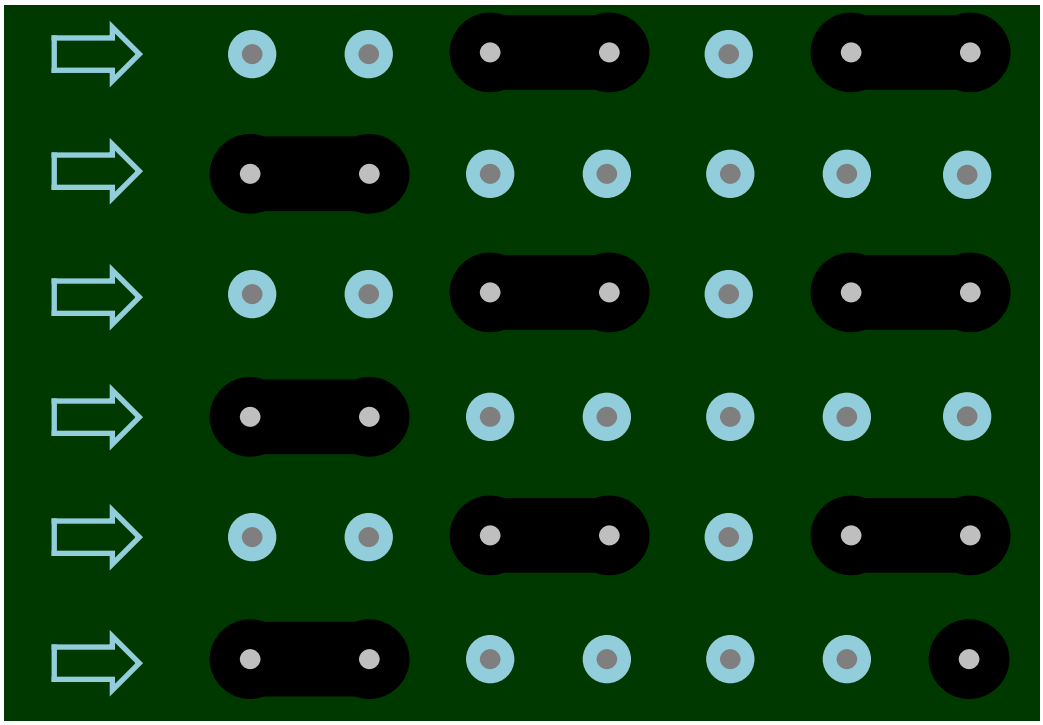
IMPORTANT! *These lanes must be maintained to allow the practical use of 1 mm pitch BGA. The vias are arranged in a 1 mm pitch manner equally spaced (see the following figure).*

Figure 6: **Lanes Maintained to Allow Practical Use of 1 mm Pitch**

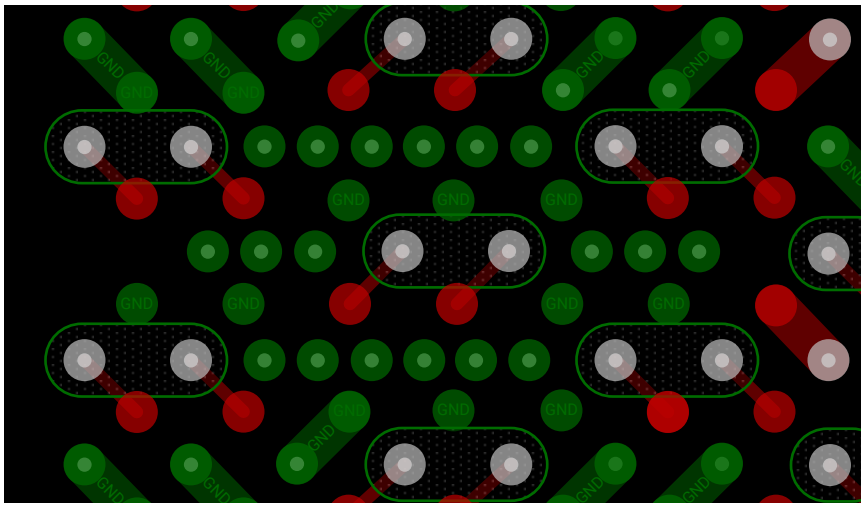


Multi Via Solution

Due to improved production processes, it is now possible to use smaller via constructions on PCBs with little increase in cost or decrease in yield.

Tighter rules for the stable manufacturing of PCBs can now be used to provide new solutions. Instead of using the *1 pin 1 via* solution, multiple smaller vias can be used in the same space. It is important to only add extra vias in a horizontal line to maintain the exit lanes for routing. Also, when possible, the pin pad size should be reduced to 80% of normal. In the example shown in the following figure, the pin pad size is reduced down to 0.4 mm/15.75th (which is also allowable for small pitch BGA devices). This creates enough room to add additional vias. If the new vias are connected to ground, the signal-to-signal cross talk is reduced. The following figure shows reduced BGA pins and via size, as well as the addition of multiple vias around a noise source signal such as a high-speed differential pair.

Figure 7: **Reduced BGA Pin and Via Size**



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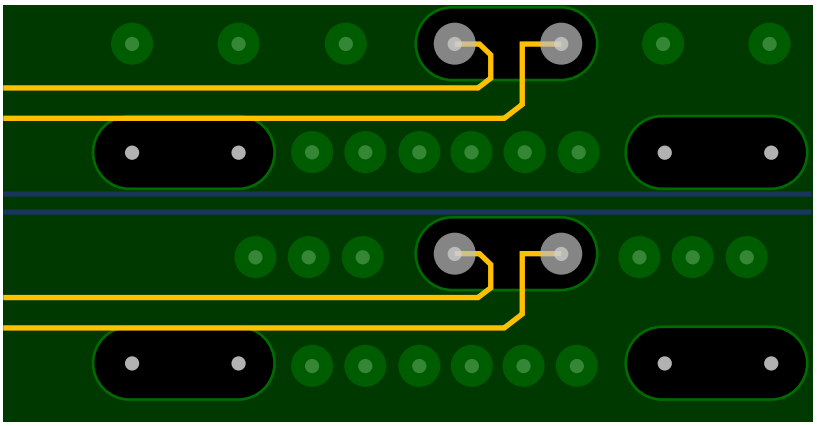
The following figure shows internal lanes that are still available for BGA breakout without breaking the design for the manufacturing rules.

Figure 8: **Internal Lanes Available for BGA Breakout**



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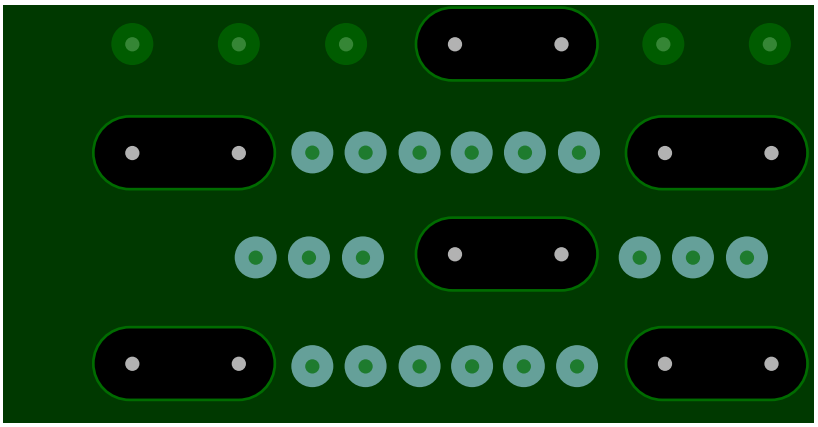
In the following figure, new ground vias are highlighted.

Figure 9: **New Ground Vias**



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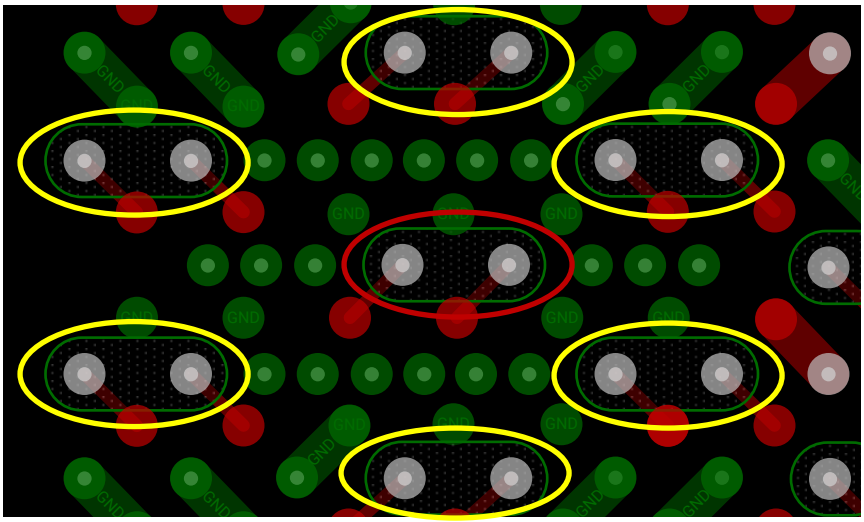
In the following figure, the pair in the red circle is the noise source and the pairs in the yellow circles are the noise recipients. There is a reduction in simulated cross talk with this method.

Figure 10: **Noise Source and Recipient**



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Simulation of Cross Talk

The simulation results show an improvement of 3.74 dB at 13.28 GHz when using the multi via solution over the standard 1 via per pad solution, as shown in the following figures. The intended use case for this example is a network card running at a data rate of 25 Gb/s. Therefore, the measurement was taken above 12.5 GHz to ensure the result is above the Nyquist frequency.

Figure 11: **Red: With GND Vias: –56.17 dB NEXT Between TX and RX**

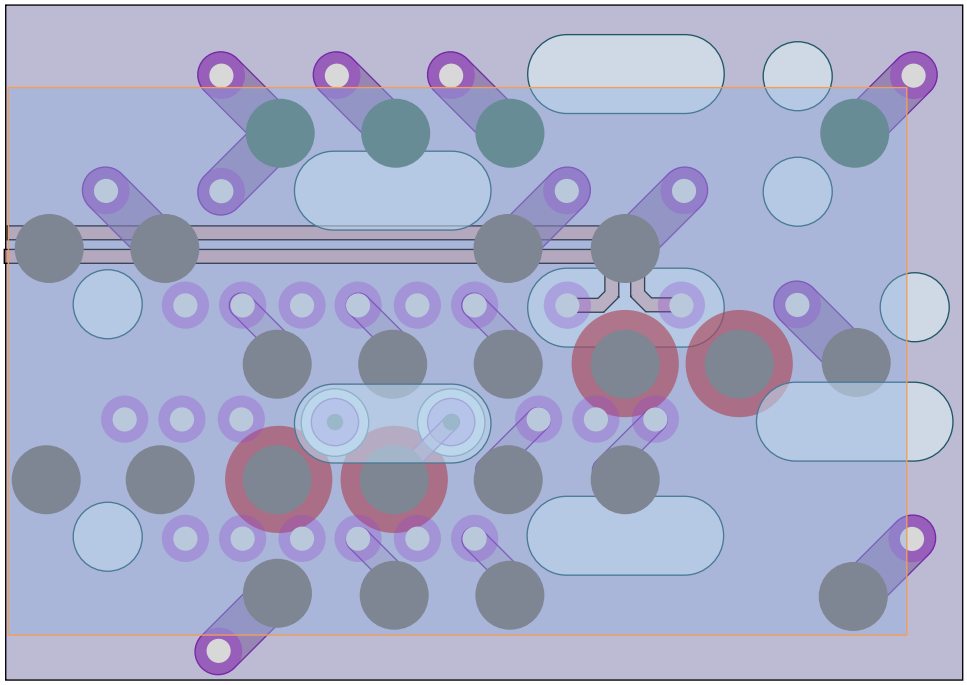

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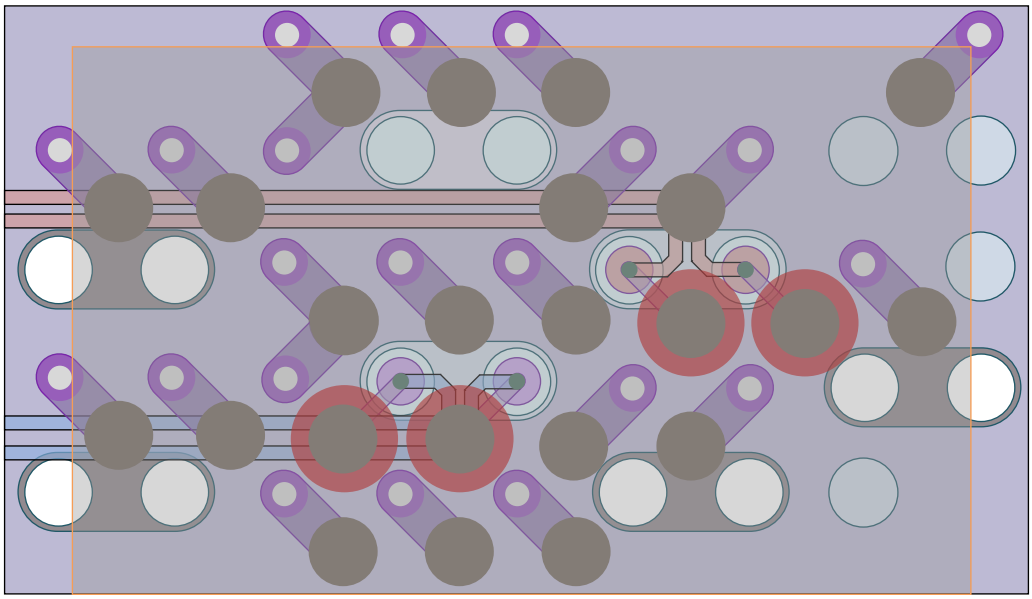
Figure 12: **Green: Without GND Vias: –52.43 dB NEXT Between TX and RX**



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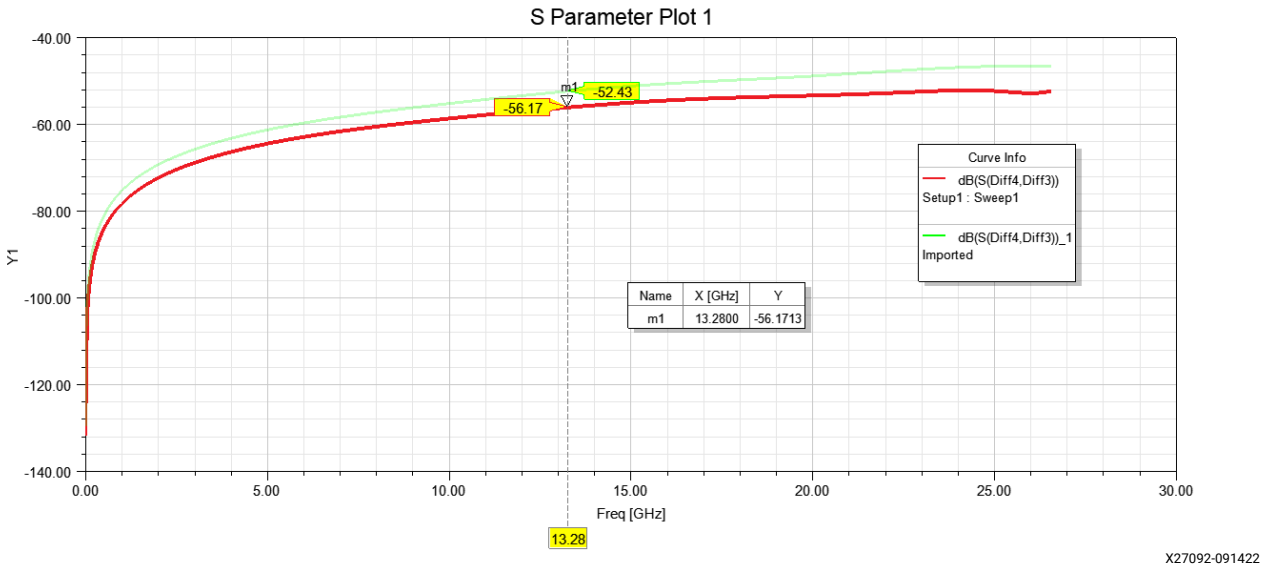
In the following figure, the green line indicates the original cross talk value when using 1 GND via per pad. Without GND vias, it is –52.43 dB NEXT between TX and RX. The red line indicates a new cross talk value when using a multiple GND via solution. With GND vias, it is –56.17 dB NEXT between TX and RX.

Figure 13: **S Parameter Plot 1**



Conclusion

This white paper outlines a technique to reduce cross talk between copper routes by reducing the impedance to ground using more local ground vias. In the example described, the simulated gain was 3.74 dB at Nyquist. The via count between routes can be maximized by the careful selection of the pad or drill size. This use case might not be suitable for all designs. Care must be taken at the design stage to ensure that the final board can be manufactured.

RECOMMENDED: *Consult your PCB manufacturing facility on current production techniques before using this solution.*

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
09/23/2022 Version 1.0	
Initial release.	N/A

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