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#### STM32WL 使用STM32CubeMX 创建LoRa 节点应用

David Liu





- 1 STM32CubeMX介绍
- 2 使用CubeMX创建LoRaWAN节点







#### STM32CubeMX介绍



#### STM32CubeMX主要功能





- ST官网下载最新版本
  - 如: STM32CubeMX 6.2.0, <u>下载</u>
- 支持跨平台运行: Windows, Linux 和 macOS
- 安装之后,按Alt+S来配置更新器—— 不仅用于GUI,还用于Cube FW库
- 选择软件库存放位置。

Get Software									
	Part Number	General Description	Software Version 🖨	Download 🖕	Previous versions				
+	STM32CubeMX-Lin	STM32Cube init code generator for Linux	6.2.0	Download	Select version $$				
+	STM32CubeMX-Mac	STM32Cube init code generator for macOS	6.2.0	Download	Select version $$				
+	STM32CubeMX-Win	STM32Cube init code generator for Windows	6.2.0	Download	Select version $$				

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Interval between two data-refreshs (days) 3	
OK	Cancel





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   可以查看支持的开发包
- 点击Refresh可以检测有无最新的开发 包,如果有可选择,然后点击Install Now





#### 开始一个STM32CubeMX工程

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#### 从MCU开始一个STM32CubeMX工程

过滤项

• 选中合适的芯片, 双击,或者点击 右上角的Start Project.

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#### 进入CubeMX界面

- ・进入STM32CubeMX工程 界面.
- 1. 进行引脚配置
- 2. 时钟树初始化
- 3. 外设配置
- 4. 中间件配置
- 5. 项目管理
- 6. 代码生成







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Series STM32WL STM32W	Lines Mcu /L5x STM32WL55JClx	Package UFBGA73	Required Peripherals None



#### 代码生成 ——选择不同的项目结构

Basic Structure: 适合没有使用中间件 或者只使用了一种中 间件的项目。用户代 码分为Src和Inc两个文 件夹,和IDE文件夹位 于同一层

Advanced Structure: 用户应用逻辑代码放 在Core文件夹下,每 个中间件的适配文件 各自放在独立的文件 夹内

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#### 代码生成 —选择不同的Cube库版本

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callback函数

#### đ MX STM32CubeMX LoRaWAN End Node.ioc: STM32WL55JClx Х F 🖸 🄰 🔆 🖅 STM32 CubeMX 10 File Window Help 1 STM32WL55JClx LoRaWAN\_End\_Node.ioc - Project Manager GENERATE CODE Home Pinout & Configuration Clock Configuration Project Manager Teele - Driver Selector Register CallBack 选择HAL或LL接口 Q Search (CrtI+F) $\odot$ $\odot$ 0 ĝ↓ 0 A. GPIO HAI ADC DISABLE DMA HAL COMP DISABLE RCC HAI CRYP DISABLE ADC DISABLE HAL DAC RTC HAI I2C DISABLE SUBGHZ HAL 12S DISABLE LoRaWAN HAL IRDA DISABLE > USART HAL LPTIM DISABLE PKA DISABLE Code Generator RNG DISABLE RTC DISABLE Generated Function Calls 2 SMARTCARD DISABLE SMBUS DISABLE Visibility (Static) DISABLE SPI SUBGHZ DISABLE MX GPIO Init GPIO 1 DISABLE $\checkmark$ $\checkmark$ TIM 2 MX DMA Init DMA $\checkmark$ UART DISABLE 3 RCC SystemClock Config $\checkmark$ USART DISABLE Δ MX ADC Init ADC $\checkmark$ ~ WWDG DISABLE 5 MX RTC Init RTC $\checkmark$ $\checkmark$ 6 SUBGHZ $\checkmark$ MX SUBGHZ Init $\checkmark$ 7 MX LoRaWAN Init LORAWAN $\checkmark$ MX USART2 UART Init USART2 $\checkmark$ 8 是否调用该函数 是否生成静态函数 是否注册对应的





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#### 如何使用STM32Cube功能扩展插件

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	► X-CUBE-MEMS1						> STMicroelectronics.X-CUBE-BLE2
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life.augmented



#### 使用CubeMX创建LoRaWAN节点



#### 开始一个LoRaWAN 节点工程

• 从MCU开始一个工程

• 从Example开始一个工程





#### 从MCU开始一个工程



#### 从MCU/开发板开始一个工程举例 (1/18)

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Other Projects		ित्			Build your certified safety system with STM32 and STM8



从MCU开始一个工程举例 (2/18)

过滤项

#### • 选中STM32WL55JC 芯片,双击

🙀 New Project from a MCU/MPU								
MCU/MPU Selector   Example S	elector Cross Selector							
MCU/MPU Filters			大日本	<u>На</u> р				
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Part Number STM32WL V	STM32WI Series							
Core ~		Sub-GHz Wireles	s Microcontrollers. D	ual-core Arn	n Cortex-M	14/M0+ @4	8 MHz w	ith 256
Chack/Unchack All	STM32WL55JC	Kbytes of Flash i modulations AF	nemory, 64 Kbytes of S 256-bit, Multiprotoco	SRAM. LOR	a, (G) FSK, ⊳Chin	(G)MSK, I	BPSK	
		modulations. AE		Ji System-O	I-Chip.			
Arm Cortex-A/ + Arm Cortex-IVI4		Unit Price for 10kU (US\$	5): 3.945		1			
Arm Cortex-M0	Product is in mass production	Boards: NUCLEO-WL55	JC - NUCLEO-WL55JC1 -	, inc.	UFBGA73			
Arm Cortex-M0+		NUCLEO-WL55JC2						
Arm Cortex-M3								
Arm Cortex-M4	The STM32WL55/54xx long-range	e wireless and ultra-low-p	ower devices embed a pow	erful and ultra-	low-power LF	WAN-compli	iant radio s	solution,
	enabling the following modulation	is: LoRa~, (G)FSK, (G)M	SK, and BPSK.					
Arm Cortex-M4 + Arm Cortex-M0+								
Arm Cortex-M4 + Arm Cortex-M0+	The LoRa <sup>®</sup> modulation is availab	le in STM32WLx5xx only.			R R			
Arm Cortex-M4 + Arm Cortex-M0+ Arm Cortex-M7 Arm Cortex-M7	The LoRa <sup>™</sup> modulation is availab These devices are designed to be	le in STM32WLx5xx only. e extremely low-power an	d are based on the high-pe	rformance Arm	® Cortex <sup>®</sup> -M	4 32-bit RISC	C core ope	rating at a
Arm Cortex-M4 + Arm Cortex-M0+ Arm Cortex-M7 Arm Cortex-M7 + Arm Cortex-M4	The LoRa <sup>®</sup> modulation is availab These devices are designed to be frequency of up to 48 MHz. This c	le in STM32WLx5xx only. e extremely low-power an core implements a full set	d are based on the high-pe of DSP instructions. It is co	rformance Arm	<sup>®</sup> Cortex <sup>®</sup> -M r an Arm <sup>®</sup> Co	4 32-bit RISC ortex <sup>®</sup> -M0+ m	C core oper icrocontrol	rating at a ller. Both
Arm Cortex-M4 + Arm Cortex-M0+ Arm Cortex-M7 Arm Cortex-M7 + Arm Cortex-M4 Arm Cortex-M33	The LoRa <sup>®</sup> modulation is availab These devices are designed to be frequency of up to 48 MHz. This of cores implement an independent	e extremely low-power an core implements a full set memory protection unit (/	d are based on the high-pe of DSP instructions. It is co MPU) that enhances the app	erformance Arm mplemented by plication securit	<sup>®</sup> Cortex <sup>®</sup> -M v an Arm <sup>®</sup> Co ty.	4 32-bit RISC ortex <sup>®</sup> -M0+ m	C core oper hicrocontrol	rating at a ller. Both
Arm Cortex-M4 + Arm Cortex-M0+ Arm Cortex-M7 Arm Cortex-M7 + Arm Cortex-M4 Arm Cortex-M33	The LoRa <sup>®</sup> modulation is availab These devices are designed to be frequency of up to 48 MHz. This c cores implement an independent	e extremely low-power an core implements a full set memory protection unit (1	d are based on the high-pe of DSP instructions. It is co MPU) that enhances the app the memory C4 (bute SDAM	erformance Arm mplemented by plication securit	<sup>®</sup> Cortex <sup>®</sup> -M v an Arm <sup>®</sup> Co ty.	4 32-bit RISC rtex <sup>®</sup> -M0+ m		rating at a ller. Both
Arm Cortex-M4 + Arm Cortex-M0+ Arm Cortex-M7 Arm Cortex-M7 + Arm Cortex-M4 Arm Cortex-M33 Series	The LoRa <sup>®</sup> modulation is availab These devices are designed to bu frequency of up to 48 MHz. This c cores implement an independent The devices ambed high encoder	e extremely low-power an core implements a full set memory protection unit (f	d are based on the high-pe of DSP instructions. It is con MPU) that enhances the app the memory of Kingto SPAM imilar items	rformance Arm mplemented by plication securit	<sup>®</sup> Cortex <sup>®</sup> -Ma 7 an Arm <sup>®</sup> Co ty.	4 32-bit RISC rtex <sup>®</sup> -M0+ m	C core oper incrocontrol	rating at a ller. Both
Arm Cortex-M4 + Arm Cortex-M0+ Arm Cortex-M7 Arm Cortex-M7 + Arm Cortex-M4 Arm Cortex-M33 Series	The LoRa <sup>®</sup> modulation is availab These devices are designed to be frequency of up to 48 MHz. This of cores implement an independent The devices are both bits aread a	e extremely low-power an core implements a full set memory protection unit (f Display s	d are based on the high-pe of DSP instructions. It is con MPU) that enhances the app the mamonic C4 (but a SPAM imilar items	rformance Arm mplemented by plication securit	<sup>®</sup> Cortex <sup>®</sup> -M- r an Arm <sup>®</sup> Co ty.	4 32-bit RISC rtex <sup>®</sup> -M0+ m		rating at a ller. Both
Arm Cortex-M4 + Arm Cortex-M0+ Arm Cortex-M7 Arm Cortex-M7 + Arm Cortex-M4 Arm Cortex-M33 Series	The LoRa <sup>®</sup> modulation is availab These devices are designed to be frequency of up to 48 MHz. This c cores implement an independent The devices or black black encoder N CUs/MPUs List: 19 items Part No Reference STM32WL54 STM32WL54C.	e extremely low-power an core implements a full set memory protection unit (f Display s Marketing × Unit Price fi Active 3.286	d are based on the high-pe of DSP instructions. It is con MPU) that enhances the app in memory of Kinto SPAM imilar items or × Board	Package     UFQFPN48	<sup>®</sup> Cortex <sup>®</sup> -M- v an Arm <sup>®</sup> Co ty. <u>Flash</u> 256 kBytes	4 32-bit RISC rrtex <sup>®</sup> -M0+ m f ophonosd l f ophonosd l responses to the second	C core oper icrocontrol	rating at a ller. Both
Arm Cortex-M4 + Arm Cortex-M0+ Arm Cortex-M7 Arm Cortex-M7 + Arm Cortex-M4 Arm Cortex-M33 Series  Arm Cortex-M33	The LoRa <sup>®</sup> modulation is availab These devices are designed to bu frequency of up to 48 MHz. This c cores implement an independent The devices ambed birth and the CUs/MPUs List: 19 items Part No Reference STM32WL54 STM32WL54C STM32WL54JC STM32WL54J	e extremely low-power an core implements a full set memory protection unit (f Display s Marketing × Unit Price f Active 3.286 Active 3.668	d are based on the high-pe of DSP instructions. It is con MPU) that enhances the app in memory of Kriste SPAM imilar items	Package     UFQFPN48     UFBGA73	<sup>®</sup> Cortex <sup>®</sup> -M- r an Arm <sup>®</sup> Co ty. <u>Flash</u> 256 kBytes 256 kBytes	4 32-bit RISC rtex <sup>®</sup> -M0+ m Contacted 1 Contacted 1 C	× 10 29 43	A MHz
Arm Cortex-M4 + Arm Cortex-M0+         Arm Cortex-M7         Arm Cortex-M7 + Arm Cortex-M4         Arm Cortex-M33         Series         Line         Package	The LoRa <sup>®</sup> modulation is availab These devices are designed to be frequency of up to 48 MHz. This c cores implement an independent The devices ambed birb encoder NCUs/MPUs List: 19 items Part No <sup>®</sup> Reference ☆ STM32WL54 STM32WL54C ☆ STM32WL54J.C STM32WL54J ☆ STM32WL55 STM32WL55C	e extremely low-power an core implements a full set memory protection unit (f Display s Marketing × Unit Price f Active 3.286 Active 3.668 Active 3.564	d are based on the high-pe of DSP instructions. It is con MPU) that enhances the app in memory of Kriste SPAM imilar items	Package     UFQFPN48     UFQGA73     UFQFPN48	<sup>®</sup> Cortex <sup>®</sup> -M- r an Arm <sup>®</sup> Co ty. <sup>®</sup> Flash 256 kBytes 256 kBytes 256 kBytes	4 32-bit RISC rtex <sup>®</sup> -M0+ m Contacted 1 Contacted 1 C	x IO 29 43 29	A SMHz 48 MHz 48 MHz 48 MHz
Arm Cortex-M4 + Arm Cortex-M0+         Arm Cortex-M7         Arm Cortex-M7 + Arm Cortex-M4         Arm Cortex-M33         Series         Line         Package         Other	The LoRa <sup>®</sup> modulation is availab These devices are designed to b frequency of up to 48 MHz. This c cores implement an independent The devices ambed birth encoder NCUs/MPUs List: 19 items Part No Reference ☆ STM32WL54 STM32WL54C ☆ STM32WL54JC STM32WL54J ☆ STM32WL55 STM32WL55C STM32WL55JC STM32WL55J	Marketing × Unit Price f Active 3.286 Active 3.564 Active 3.945	d are based on the high-pe of DSP instructions. It is co MPU) that enhances the app in mamory C4 Kbite SPAM imilar items orX Board	Package     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFQGA73     UFBGA73	<ul> <li>Cortex<sup>®</sup>-M- r an Arm<sup>®</sup> Co ty.</li> <li>Flash</li> <li>256 kBytes</li> <li>256 kBytes</li> <li>256 kBytes</li> <li>256 kBytes</li> <li>256 kBytes</li> </ul>	4 32-bit RISC rtex <sup>®</sup> -M0+ m 20 kBytes 64 kBytes 64 kBytes 64 kBytes	× 10 29 43 29 43	Arating at a ller. Both Export Kereg. X 48 MHz 48 MHz 48 MHz 48 MHz 48 MHz
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□ Arm Cortex-M4 + Arm Cortex-M0+         □ Arm Cortex-M7         □ Arm Cortex-M7 + Arm Cortex-M4         □ Arm Cortex-M33         Series       >         Line       >         Package       >         Other       >         Peripheral       ✓	The LoRa <sup>®</sup> modulation is availab These devices are designed to b frequency of up to 48 MHz. This c cores implement an independent The devices ambed bids aread a N CUs/MPUs List: 19 items Part No Reference ☆ STM32WL54 STM32WL54C ☆ STM32WL54 STM32WL54J ☆ STM32WL55 STM32WL55J STM32WL55 STM32WL55J STM32WL55 STM32WL55J ☆ STM32WL55 STM32WL55J ☆ STM32WL55 STM32WL55J ☆ STM32WL55 STM32WL55J ☆ STM32WL55 STM32WL55J	Marketing × Unit Price f Marketing × Unit Price f Active 3.286 Active 3.668 Active 3.564 Active 3.945 Active 3.945 NA NA NA	d are based on the high-pe of DSP instructions. It is co MPU) that enhances the app in memory C4 Kbite SPAM imilar items orX Board	Package     UFQFPN48     UFQFPN48     UFQFPN48     UFQGA73     UFBGA73     UFBGA73     WLCSP59     UFQFPN48	<ul> <li>Cortex<sup>®</sup>-M- ran Arm<sup>®</sup> Co ty.</li> <li>Flash</li> <li>256 kBytes</li> <li>266 kBytes</li> </ul>	4 32-bit RISC rtex <sup>®</sup> -M0+ m 20 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes	× 10 29 43 29 43 22 29	A S MHZ 48 MHZ 48 MHZ 48 MHZ 48 MHZ 48 MHZ 48 MHZ 48 MHZ 48 MHZ
Arm Cortex-M4 + Arm Cortex-M0+ Arm Cortex-M7 Arm Cortex-M7 + Arm Cortex-M4 Arm Cortex-M33 Series  Package  Package  Package  Other  Peripheral  OLDC 12 bit OL 12 bit OL 12	The LoRa <sup>®</sup> modulation is availab These devices are designed to b frequency of up to 48 MHz. This c cores implement an independent The devices ambed bids aread a NCUs/MPUs List: 19 items Part No Reference ☆ STM32WL54 STM32WL54C. ☆ STM32WL54 STM32WL54J ☆ STM32WL55 STM32WL55J STM32WL55 STM32WL55J STM32WL55 STM32WL55J STM32WL55 STM32WL55J ☆ STM32WL55 STM32WL55J ☆ STM32WL55 STM32WL55J ☆ STM32WL54 STM32WL55J ☆ STM32WLE4 STM32WLE4 ☆ STM32WLE4 STM32WLE4	le in STM32WLx5xx only. e extremely low-power an core implements a full set memory protection unit (f Display s Marketing × Unit Price f Active 3.286 Active 3.668 Active 3.564 Active 3.945 NA NA NA NA	d are based on the high-pe of DSP instructions. It is co MPU) that enhances the app in memory C4 Kbite SPAM imilar items orX Board	Package     VFQFPN48     UFQFPN48     UFQFPN48     UFQGA73     UFQGA73     WLCSP59     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48	<ul> <li>Cortex<sup>®</sup>-M- r an Arm<sup>®</sup> Co ty.</li> <li>Flash</li> <li>256 kBytes</li> <li>256 kBytes</li> <li>256 kBytes</li> <li>256 kBytes</li> <li>256 kBytes</li> <li>256 kBytes</li> <li>128 kBytes</li> <li>128 kBytes</li> </ul>	4 32-bit RISC rtex <sup>®</sup> -M0+ m 20 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes	× 10 29 43 29 43 22 29 29	A S MHZ 48 MHZ 48 MHZ 48 MHZ 48 MHZ 48 MHZ 48 MHZ 48 MHZ 48 MHZ 48 MHZ
□ Arm Cortex-M4 + Arm Cortex-M0+         □ Arm Cortex-M7         □ Arm Cortex-M7 + Arm Cortex-M4         □ Arm Cortex-M33         Series       >         Line       >         Package       >         Other       >         Peripheral       ~         Ø ADC 12-bit       0       12	The LoRa <sup>®</sup> modulation is availab These devices are designed to b frequency of up to 48 MHz. This c cores implement an independent The devices ambed bids aread a NCUs/MPUs List: 19 items Part No Reference ☆ STM32WL54 STM32WL54C. ☆ STM32WL54 STM32WL54J ☆ STM32WL55 STM32WL55J STM32WL55 STM32WL55J STM32WL55 STM32WL55J ☆ STM32WL55 STM32WL55J ☆ STM32WL55 STM32WL55J ☆ STM32WL54 STM32WL54 ☆ STM32WLE4 STM32WLE4 ☆ STM32WLE4 STM32WLE4	le in STM32WLx5xx only. e extremely low-power an core implements a full set memory protection unit (f Display s Marketing × Unit Price f Active 3.286 Active 3.668 Active 3.945 NA NA NA NA NA NA NA NA Active 2.777	d are based on the high-pe of DSP instructions. It is co MPU) that enhances the app in memory C4 Kbite SPAM imilar items orX Board	Package     VFQFPN48     UFQFPN48     UFQFPN48     UFBGA73     UFQFPN48     UFBGA73     WLCSP59     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48	<ul> <li>Cortex<sup>®</sup>-M- r an Arm<sup>®</sup> Co ty.</li> <li>Flash</li> <li>256 kBytes</li> </ul>	4 32-bit RISC rtex <sup>®</sup> -M0+ m 20 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes 64 kBytes	× 10 29 43 29 43 22 29 29 29 29	A S MHZ 48 MHZ
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□ Arm Cortex-M4 + Arm Cortex-M0+         □ Arm Cortex-M7         □ Arm Cortex-M7 + Arm Cortex-M4         □ Arm Cortex-M33         Series       >         Line       >         Package       >         Other       >         Peripheral       ~         ØADC 12-bit       0       12         ØADC 16-bit       0       0         ØADC 16-bit       0       1         ØADC 16-bit       0       1         ØADC 16-bit       0       0         ØADC       0       0	The LoRa <sup>®</sup> modulation is availab These devices are designed to b frequency of up to 48 MHz. This c cores implement an independent The devices ambed bids encode NCUs/MPUs List: 19 items Part No Reference ☆ STM32WL54 STM32WL542 ☆ STM32WL55 STM32WL542 ☆ STM32WL55 STM32WL552 ③ STM32WL55 STM32WL552 ③ STM32WL55 STM32WL552 ③ STM32WL55 STM32WL552 ☆ STM32WL55 STM32WL552 ☆ STM32WL54 STM32WL54 ☆ STM32WLE4 STM32WLE4 ☆ STM32WLE4 STM32WLE4	le in STM32WLx5xx only. e extremely low-power an core implements a full set memory protection unit (f Display s Marketing × Unit Price f Active 3.286 Active 3.668 Active 3.564 Active 3.945 NA NA NA NA NA NA Active 2.777 NA NA NA NA Active 3.159	d are based on the high-pe of DSP instructions. It is co MPU) that enhances the app in mamory C4 Kbits SPAM imilar items orX Board	Package     VFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFBGA73     WLCSP59     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFQA73     UFBGA73     UFBGA73	<ul> <li>Cortex<sup>®</sup>-M- r an Arm<sup>®</sup> Co ty.</li> <li>Flash</li> <li>256 kBytes</li> </ul>	4 32-bit RISC rttex <sup>®</sup> -M0+ m 20 kBytes 64	x 10 29 43 29 43 29 43 29 43 29 43 29 29 29 29 29 29 29 43 43 43	A S MHZ A S MHZ
□ Arm Cortex-M4 + Arm Cortex-M0+         □ Arm Cortex-M7         □ Arm Cortex-M7 + Arm Cortex-M4         □ Arm Cortex-M33         Series       >         Line       >         Package       >         Other       >         Peripheral       ~         ØADC 12-bit       0       12         ØADC 16-bit       0       0         ØADC 16-bit       0       1         ØADC 16-bit       0       1         ØADC 16-bit       0       2         ØADC 16-bit       0       2         ØADC 16-bit       0       2	The LoRa <sup>®</sup> modulation is availab These devices are designed to b frequency of up to 48 MHz. This of cores implement an independent The divides onebod bids encoder NCUs/MPUs List: 19 items Part No Reference ☆ STM32WL54 STM32WL54C. ☆ STM32WL54 STM32WL54 ☆ STM32WL55 STM32WL54 ☆ STM32WL55 STM32WL54 ☆ STM32WL55 STM32WL55 ③ STM32WL55 STM32WL55 ☆ STM32WLE4 STM32WLE4 ☆ STM32WLE4 STM32WLE4	le in STM32WLx5xx only. e extremely low-power an core implements a full set memory protection unit (f Display s Marketing × Unit Price f Active 3.286 Active 3.668 Active 3.564 Active 3.945 NA NA NA NA NA NA NA NA Active 2.777 NA NA Active 3.159 Active 2.545	d are based on the high-pe of DSP instructions. It is co MPU) that enhances the app in mamory C4 Kbits SPAM imilar items orX Board NUCLEO_NUCLEO_NUCLE	Package     VFQFPN48     UFQFPN48     UFQA73     UFBGA73     UFBGA73     UFBGA73	<ul> <li>Cortex<sup>®</sup>-M- r an Arm<sup>®</sup> Co ty.</li> <li>Flash</li> <li>256 kBytes</li> <li>4 kBytes</li> <li>256 kBytes</li> <li>4 kBytes</li> <li>256 kBytes</li> <li>4 kBytes</li> </ul>	4 32-bit RISC rttex <sup>®</sup> -M0+ m 20 kBytes 64 kBytes 20 kBytes 20 kBytes 20 kBytes	× 10 29 43 29 43 29 43 29 43 29 29 29 29 29 29 43 43 43 43 29	A S MHZ A S MHZ
□ Arm Cortex-M4 + Arm Cortex-M0+         □ Arm Cortex-M7         □ Arm Cortex-M7 + Arm Cortex-M4         □ Arm Cortex-M33         Series       >         Line       >         Package       >         Other       >         ØADC 12-bit       0       12         ØADC 16-bit       0       0         ØADC 16-bit       0       1         ØADC 16-bit       0       0         ØADS       0       1         ØADS       0       0         ØADS       0       0         ØADS       0       0	The LoRa <sup>®</sup> modulation is availab These devices are designed to b frequency of up to 48 MHz. This c cores implement an independent The devices ambed bids exceed a NCUs/MPUs List: 19 items <sup>↑</sup> Part No Reference ☆ STM32WL54 STM32WL54C. ☆ STM32WL55 STM32WL54J ☆ STM32WL55 STM32WL55C. ③ STM32WL55 STM32WL55J ☆ STM32WL55 STM32WL55J ☆ STM32WLE4 STM32WLE4 ☆ STM32WLE5 STM32WLE5 ☆ STM32WLE5 STM32WLE5	le in STM32WLx5xx only. e extremely low-power an core implements a full set memory protection unit (f Display s Marketing × Unit Price f Active 3.286 Active 3.668 Active 3.564 Active 3.945 NA NA NA NA NA NA NA NA Active 2.777 NA NA Active 3.159 Active 2.73	d are based on the high-pe of DSP instructions. It is co MPU) that enhances the app in mamory of Kbute SPAM imilar items orX Board NUCLEO_NUCLEO_NUCLE	Package     VFQFPN48     UFQFPN48     UFBGA73     UFBGA73     UFBGA73     UFBGA73	<ul> <li>Cortex<sup>®</sup>-M- r an Arm<sup>®</sup> Co ty.</li> <li>Flash</li> <li>256 kBytes</li> <li>256 kBytes</li> <li>256 kBytes</li> <li>256 kBytes</li> <li>256 kBytes</li> <li>256 kBytes</li> <li>128 kBytes</li> </ul>	4 32-bit RISC rttex <sup>®</sup> -M0+ m 20 kBytes 64	x 10 29 43 29 43 29 43 29 43 29 29 29 29 29 29 29 43 43 43 43 29 29 29 29 29 29 29 29 29 29 29 29 29	A S MHZ A S MHZ
□ Arm Cortex-M4 + Arm Cortex-M0+         □ Arm Cortex-M7         □ Arm Cortex-M7 + Arm Cortex-M4         □ Arm Cortex-M33         Series       >         Line       >         Package       >         Other       >         ØADC 12-bit       0       12         ØADC 16-bit       0       0         ØAES       0       1         ØCAN       0       0         ØCORDIC       0       0         ØCADC 12-bit       0       0	The LoRa <sup>®</sup> modulation is availab         These devices are designed to b         frequency of up to 48 MHz. This c         cores implement an independent         The dovices ambed birb encode         M CUs/MPUs List: 19 items         Image: STM32WL54 STM32WL54C.         Image: STM32WL55 STM32WL54J         STM32WL55 STM32WL55C.         STM32WL55 STM32WL55J         STM32WL55 STM32WL55J         STM32WL55 STM32WL55J         STM32WL64         STM32WLE4         STM32WLE5         STM32WLE5         STM32WLE5         STM32WLE5         STM32WLE5         STM32WLE5         STM32WLE5     <	le in STM32WLx5xx only. e extremely low-power an core implements a full set memory protection unit (f Display s Marketing × Unit Price f Active 3.286 Active 3.668 Active 3.564 Active 3.945 NA NA NA NA NA NA NA NA Active 2.777 NA NA Active 3.159 Active 2.73 Active 2.73 Active 3.054	d are based on the high-pe of DSP instructions. It is con MPU) that enhances the app initial ritems orX Board NUCLEO_NUCLEO_NUCLE NUCLEO_NUCLEO_NUCLE	Package     VFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFQFPN48     UFQA73     UFBGA73     UFBGA73     UFBGA73     UFBGA73     UFBGA73     UFBGA73	<ul> <li>Cortex<sup>®</sup>-M- r an Arm<sup>®</sup> Co ty.</li> <li>Flash</li> <li>256 kBytes</li> </ul>	4 32-bit RISC rttex <sup>®</sup> -M0+ m 20 kBytes 64	x 10 29 43 29 43 29 43 29 29 29 29 29 29 29 43 43 43 43 29 29 29 29 29 29 29 29 29 29 29 29 29	A solution of the second of th



#### 从MCU开始一个工程举例 (3/18)

 选择as Single core project,点击OK





#### 从MCU开始一个工程举例 (4/18)

Pinout & Configuration Clock Configuration Software Packs RCC Mode and Configuration 0  $\sim$ 3 A->Z Mode High Speed Clock (HSE) TCXO  $\sim$ System Core ow Speed Clock (LSE) Crystal/Ceramic Resonato Master Clock Output DMA GPIO LSCO Clock Output HSEM Audio Clock Input (I2S\_CKIN) IWDG NVIC WWDG Analog 5  $\sim$ Timers Configuration LPTIM1 LPTIM2 LPTIM3 Parameter Settings User Constants A RTC A TIM1 Configure the below parameters A TIM2 Q Search (CrtI+F) 0 TIM16 System Parameters TIM17 VDD voltage (V) 3.3 V Instruction Cache Enabled Prefetch Buffer Disabled 4 Connectivity Data Cache Enabled ٠ Flash Latency(WS) 2 WS (3 CPU cycle) 12C1 V RCC Parameters 12C2 64 HSI Calibration Value 12C3 MSI Calibration Value 0 MSI Auto Calibration Disabled LPUART1 HSE Startun Timout Value (ms) 100 CDH

- 开始外设配置:
  - 1. 配置RCC:
    - HSE:TCXO
    - LSE:Crystal/Ceramic Resonator



### 从MCU开始一个工程举例 (5/18)



- 开始外设配置 2.RTC配置
  - RTC Clock Mux选择LSE



### 从MCU开始一个工程举例 (6/18)





从MCU开始一个工程举例(7/18)



#### • 开始外设配置 3.使能ADC



#### 从MCU开始一个工程举例 (8/18)

Pinout & Configuration **Clock Configuration** 1 ✓ Software Packs 🗸 Pi Ô USART2 Mode and Configuration 0  $\sim$ A->Z Mode 3 Mode Asynchronous  $\sim$ System Core 5 Hardware Flow Control (RS232) Disable 1.1 > Analog Hardware Flow Control (RS485) Slave Select(NSS) Management Disable > Timers  $\sim$ Connectivity ۰ I2C1 12C2 12C3 LPUART1 Configuration SPI1 SPI2 SUBGHZ USART1 NVIC Settings OMA Settings GPIO Settings ▲ USART2 Parameter Settings User Constants Δ remove Search (CrtI+F) > Multimedia Constant Value Constant Name RTC N PREDIV S 10 >Security RTC PREDIV S ((1<<RTC N PREDIV S)-1) RTC PREDIV A ((1<<(15-RTC N\_PREDIV S))-1) Computing > (5) USART BAUDRATE 115200 Middleware  $\sim$ 

• 开始外设配置 4.配置USART2



#### 从MCU开始一个工程举例 (9/18)



### 从MCU开始一个工程举例 (10/18)



life.augmented

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### 从MCU开始一个工程举例 (11/18)

1 按键控制的GPIO





5.配置BUT,LED,DBG, RF\_CTRL GPIO.

STM32WL Nucleo 板上对应线路参考。



#### 3 DBG 的GPIO

	T SWDIO	PA13	B8	1412
T SWDIO	× T_SWOLK	DA14	4.4	PA13
TSWCIK		PA14	A4	DA 14
1 SWCLK	T JTDI	PA15	B3	TAIT
T JIDI	* *			PA15





# 从MCU开始一个工程举例 (12/18)

Clock Configuration Pinout & Configuration 1 ✓ Software Packs ٢ SUBGHZ Mode and Configuration  $\sim$ A->Z Mode 3 COMP2 Activated DAC VREFBUF Timers  $\sim$ ۰ LPTIM1 LPTIM2 LPTIM3 RTC TIM1 TIM2 TIM16 TIM17 Configuration Connectivity  $\sim$ 3 ..... I2C1 Parameter Settings NVIC 12C2 Sub Priority 12C3 SUBGHZ Radio Interrupt 4 4 LPUART1 SPI1 2 CDP SUBGHZ USART2

• 开始外设配置 6.使能SUGBHZ



### 从MCU开始一个工程举例 (13/18)

• 开始外设配置 7.Middleware 选择LoRaWAN





#### 从MCU开始一个工程举例 (14/18)



# • 开始外设配置

LoRaWAN commissioning	LoRaWAN middleware	User Constants	Platform Settings
	LoRaWAN application		
o figure the below parameters :			
Q Search (CrtI+F) ③ ③			0
Region(s) selection	please select	the deaired region(s) in t	the list below
Region Asia freq: 923			
Region Australia freq: 915			
Region China freq: 470			
Region China freq: 779			
Region Europe freq: 433			
Region Europe freq: 868	<b>.</b>		
Region Korea freq: 920			
Region India freq: 865			
Region USA freq: 915	<b>.</b>		
Region Russia freq: 864			
Enable Hybrid mode			
Enable LoRaMAC ClassB			
radio_board_if			
Radio maximum wakeup time (in ms	) 10		
TCXO support	<b>v</b>		
DCDC support	<b>S</b>		
Activate Radio Board Interface	<b>S</b>		
Activate Debug Line	<b>2</b>		
<pre> mw_log_conf </pre>			
Enable Middleware log	<b>S</b>		

LoRaW	AN application 🛛 © LoRaWAN commissioning 🔍 LoRaWAN middleware 🔍 User	Constants Sett	ings	
Platform pro	posal			
Name	IPs or Components	Found Solutions		BSP API
LED 3	GPIO:Output ~	PB11 [LED3]	~ ~	Unknown
LED 2	GPIO:Output ~	PB9 [LED2]	~	Unknown
LED 1	GPIO:Outout ~	PB15 ILED11	~	Unknown
BUTTON 1		PA0 (BUT1)		Unknown
BUTTON		PAU[BUT1]	· · · · · · · · · · · · · · · · · · ·	Unknown
BUTTON 3	GPI0:EXII ~	PC6 [BU13]	~ ~	Unknown
BUTTON 2	GPIO:EXTI V	PA1 [BUT2]	V	Unknown
Radio				
Name	IPs or Components	Found Solutions		BSP API
RF SW CT	RL 3 GPI0:Output	PC3 [RF_CTRL3]	~	Unknown
RF SW CT	RL 1 GPI0:Output	V PC4 [RF_CTRL1]	~ ~	Unknown
RF SW CT	RL 2 GPI0:Output	V PC5 [RF_CTRL2]	~	Unknown
Name	IPs or Components	Found Solutions		BSP API
Debug Line	1 GPIO:Output	Undefined		Unknown
Debug Line	2 GPIO-Output	Undefined		Unknown
Debug Line	2 0710-04694	Undefined	· · · · · · · · · · · · · · · · · · ·	Uningen
Line	s jonio.output		`	UNKNOWN
Debug Line	4 GPI0:Output	Undefined	V	Unknown
11.				



#### 从MCU开始一个工程举例(15/18)

• 完成配置 8. 工程选项

Home > STM32W	/L55JClx 🔰 LoRaWAN_End_nod	e demo.ioc - Project Manager >		GENERATE CODE
Pinout	& Configuration	Clock Configuration	Project Manager	Tools
Project	Project Settings Project Name LoRaWAN End node demo Project Location C:Work\STM32WL\STM32WL Project Application Structure	STM32WL CubeMx project		
Code Generator	Advanced Toolchain Folder Location C:Work\STM32WL\STM32WL Project Toolchain / IDE N EWARM	Do not generate the main()  ISTM32WL CubeMx project\LoRaWAN_End_node demo\ In Version B      Generate Under Root		
Advanced Settings	Linker Settings Minimum Heap Size 0x200 Minimum Stack Size 0x800	6		
	Mcu and Firmware Package Mcu Reference STM32WL55JCtx Firmware Package Name and Version STM32Cube FW_WL V1.0.0	7		
	Use Default Firmware Location	ory/STM32Cube_FW_WL_V1.0.0 Brow	se	



### 从MCU开始一个工程举例(16/18)

• 完成配置 8. 工程选项

8

Home $>$ STM32WL55JClx $>$ LoRaWAN_End_node demo.ioc - Project Manager $>$						
Pinout 8	Configuration	Clock Configuration	Pro	oject Manager		
Project	<ul> <li>STM32Cube MCU packages and</li> <li>Copy all used libraries into th</li> <li>Copy only the necessary library files a</li> </ul>	embedded software packs ne project folder ary files s reference in the toolchain project configuration file	9			
	Generated files			)		
Code Generator	<ul> <li>Generate peripheral initializa</li> <li>Backup previously generated</li> <li>Keep User Code when re-gen</li> <li>Delete previously generated</li> </ul>	tion as a pair of '.c/.h' files per peripheral I files when re-generating nerating files when not re-generated				
	HAL Settings Set all free pins as analog (to Enable Full Assert	o optimize the power consumption)				
Advanced Settings	Template Settings Select a template to generate cu	istomized code	Settings			



#### 从MCU开始一个工程举例 (17/18)

• 生成代码 9.点击右上角 GENERATE CODE

Home $>$ STM32WL55JCIX $>$ LoRaWAN_End_node demo.ioc - Project Manager $>$							
Pinout 8	Configuration	Clock Configur	ration	Project I	Manager	Tools	
Project	STM32Cube MCU packages and Copy all used libraries into th Copy only the necessary libra Add necessary library files as	embedded software packs e project folder ary files reference in the toolchain project co	onfiguration file				
Code Generator	Generate peripheral initializat Backup previously generated Keep User Code when re-gen Delete previously generated fi (HAL Settings	ion as a pair of '.c/.h' files per periphe files when re-generating erating les when not re-generate	eral Ig user source code				
Advanced Settings	Central free pins as analog (to     Central free pins as anal	optimize the power consumption)		Settings			



1

### 从MCU开始一个工程举例 (18/18)

- 完成应用代码
  - MX\_LoRaWAN\_Init()
  - MX\_LoRaWAN\_Process()

etc

rkspace 👻 J	I ×     main.c     x     app_lorawan.c     lora_app.c
RaWAN_End_node demo	main()
iles 🔅	84 /* USER CODE END SysInit */
■LoBaWAN End node demo-LoBa	
	86 2A Initialize all configured peripherals */
	88 /* USED CODE RECIA 2 */
u startup stm32wl55∞ cm4 s	89
	90 /* USER CODE END 2 */
	91
	92 /* Infinite loop */
L⊕ STM32WL∞ HAL Driver	93 /* USER CODE BEGIN WHILE */
E Middlewares	94 while (1)
- 🗉 🛋 LoRaWAN	95 🗗 {
- ⊕ ■ SubGHz Phv	96 /* USER CODE END WHILE */
- Utilities	97 MX_LoRaWAN_Process();
- 🗉 🖬 Output	
	100 - 100 -
	$100 \qquad \}$
	103
	104 🖂 /**
oRaWAN End node demo	
d	
Mossagos	
messages	





#### 从Example开始一个工程



#### 从Example开始一个工程(1/8)

MX STM32CubeMX Untit	led				$ \Box$ $\times$
	File	Window	Help		💿 🖪 🖻 🎽 🔆 🏹
Home >					
Existing Projects			New Project		Manage software installations
Recent Opened Proje	ects		I need to :		Check for STM32CubeMX and embedded software package
SubGHz_Phy_Ping Last modified date : 28/3	Pong.ioc 10/2020 16:29:26	MX	Start My project from M	<u>ACU</u>	CHECK FOR UPDATES
LoRaWAN_End_no	ode demo.ioc 03/2021 15:35:48	MX	ACCESS TO MCU SE		Install or remove embedded software packages
LoRaWAN_End_No Last modified date : 18/0	ode.ioc 03/2021 16:24:24	MX	ACCESS TO BOARD S	ELECTOR	
LoRaWAN_End_No	bde.ioc <mark> </mark>	™ 好	Start My project from E	Example SELECTOR	SIL ASIL ClassB Partner Program
Last modified date : 17/0	03/2021 17:37:57				Ready Ready Ready
Other Projects		दि			Build your certified safety system with STM32 and STM8
					About STM32 🛛 🖌 External Tools



#### 从Example开始一个工程(2/8)

- 根据demo板选择合适的 例程
- 这里选择NUCLEOWL55JC1

LoRaWAN\_End\_Node





# 从Example开始一个工程(3/8)

- 点击右上角Start Project
- 选择路径以及合适的编译器,

比如选择IAR





# 从Example开始一个工程(4/8)

点击OK,后会自动打开
 Example的IAR工程

Project - IAR Embedded Workbench	IDE - Arm	8.50.9 —		×
File Edit View Project ST-Link To	ools Win	dow Help		
🔁 🖻 🖬 🖶 🛛 🖉 📋	5 C	- < Q > 🔩 HE < Q > 🖬 🗈 🗈 🗈 🖉 🖛 💽 🖉		
Workspace 🗸	, ų Χ	main.c app_lorawan.c x		-
LoRaWAN_End_Node	~ 1	IX_LoRaWAN_Init()		f
Files       Image: Core state st	•	<pre>60 61 /* Exported functions 62 63 void MX_LORaWAN_Init(void) 64 = { 65 /* USER CODE BEGIN MX_LORaWAN_Init_1 */ 66 67 /* USER CODE END MX_LORaWAN_Init_1 */ 68 SystemApp_Init(); 69 /* USER CODE BEGIN MX_LORaWAN_Init_2 */ 70 71 /* USER CODE END MX_LORaWAN_Init_2 */ 72 LORaWAN_Init(); 73 /* USER CODE BEGIN MX_LORaWAN_Init_3 */ 74 75 /* USER CODE END MX_LORAWAN_Init_3 */</pre>	*/	
LoRaWAN_End_Node		76 } 77 78 void MX_LoRaWAN_Process(void) 79  { 80 /* USER CODE BEGIN MX_LoRaWAN_Process 1 */ <		> ~



# 从Example开始一个工程(5/8)

 在安装文件路径.ioc的 STM32CubeMX应用文件

STM32WL Project > STM32WL CubeMx project > LoRaWAN_End_Node >					
Name	Date modified	Туре			
Core	11/11/2020 8:50 AM	File folder			
Drivers	3/26/2021 4:45 PM	File folder			
EWARM	3/26/2021 4:46 PM	File folder			
LoRaWAN	11/11/2020 8:50 AM	File folder			
MDK-ARM	3/26/2021 4:45 PM	File folder			
Middlewares	3/26/2021 4:45 PM	File folder			
STM32CubeIDE	3/26/2021 4:45 PM	File folder			
Utilities	11/11/2020 8:50 AM	File folder			
LoRaWAN_End_Node.ioc	3/26/2021 4:45 PM	STM32CubeMX			
readme.txt	11/11/2020 8:50 AM	Text Document			



### 从Example开始一个工程(6/8)

- 点击打开.ioc文件
- 客户可以在example的基础上 增删外设,或添加应用





### 从Example开始一个工程(7/8)

#### • 生成代码 点击右上角 GENERATE CODE

Home 🔰 STM32W	/L55JCIx 🔰 LoRaWAN_End_I	node demo.ioc - Project Manager >		GENERATE CODE
Pinout 8	Configuration	Clock Configuration	Project Manager	Tools
Project	STM32Cube MCU packages and er O Copy all used libraries into the O Copy only the necessary library Add necessary library files as r Generated files	mbedded software packs project folder y files eference in the toolchain project configuration file		
Code Generator	<ul> <li>Generate peripheral initializatio</li> <li>Backup previously generated fil</li> <li>Keep User Code when re-gener</li> <li>Delete previously generated file</li> </ul>	n as a pair of '.c/.h' files per peripheral es when re-generating rating s when not re-generate		
Advanced Settings	HAL Settings Set all free pins as analog (to o Enable Full Assert Template Settings Select a template to generate cust	ptimize the power consumption)	Settings	



# 从Example开始一个工程(8/8)

• 完成应用代码

Project - IAR Embedded Workber	nch I	DE - Ai	rm 8.50.9 —		×	
	)   ;		vindow Help → < Q > \$\$ ► = < Q > \$ D   0 = 0 ► ] =			
Workspace	-	ąχ	main.c app_lorawan.c ×			•
LoRaWAN_End_Node		~	MX_LoRaWAN_Init()			f(
Files  Core  Files  Files  Core  Files  Files Files Files  Files  Files Files  Files Files Files Files Files Files Files Files Files Files Files Files Files Files Files Files Files Files File	<b>Ö</b>	•	<pre>60 61 /* Exported functions 62 63 void MX_LoRaWAN_Init(void) 64 65 /* USER CODE BEGIN MX_LORaWAN_Init_1 */ 66 /* USER CODE END MX_LORaWAN_Init_1 */ 68 SystemApp_Init(); 69 /* USER CODE BEGIN MX_LORaWAN_Init_2 */ 70 /* USER CODE BEGIN MX_LORaWAN_Init_2 */ 71 LoRaWAN_Init(); 73 /* USER CODE BEGIN MX_LORaWAN_Init_3 */ 74 /* USER CODE BEGIN MX_LORaWAN_Init_3 */ 75 /* USER CODE END MX_LORaWAN_Init_3 */ 76 }</pre>	*/		^
LoRaWAN_End_Node			78 void MX_LoRaWAN_Process(void) 79 - { 80 /* USER CODE BEGIN MX LORAWAN Process 1 */ <		>	~











#### 1. STM32CubeMX介绍

#### 2. 使用CubeMX创建LoRaWAN节点

- 从MCU开始一个工程
- 从Example开始一个工程





Help		
Help	F1	
About	Alt-A	
Docs & Resources	Alt-D	
Tutorial Videos	Alt-V	
Refresh Data		
User Preferences		
Check for Updates		
Manage embedded software packages		
Updater Settings	Alt-S	





#### 用户手册/应用笔记

用户手册/应用笔记					
<u>UM1718</u>	STM32CubeMX for STM32 configuration and initialization C code generation 《使用STM32CubeMX对STM32进行配置以及生成初始化代码》				
<u>UM2739</u>	How to create a software pack enhanced for STM32CubeMX using STM32 Pack Creator tool 《如何使用STM32Pack Creator工具生成STM32CubeMX的插件包》				
<u>AN5418</u>	How to build a simple USB-PD sink application with STM32CubeMX 《使用STM32CubeMX构建一个简单的USB-PD接收器应用程序》				
<u>AN5426</u>	Migrating graphics middleware projects from STM32CubeMX 5.4.0 to STM32CubeMX 5.5.0 《将图形中间组件从STM32CubeMX5.4.0移植到STM32CubeMX5.5.0》				



# Thank you

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