Data Sheet

Heracles:

Automated SI Signoff for High Speed Design

Crosstalk and impedance analysis for high speed PCB design becomes more and more important due to the high data rate and tightly coupled routing. Traditional circuit-based analysis can not meet the accuracy demand. Three-dimensional (3D) full-wave electromagnetic solver is required to capture the complex 3D PCB environment and the frequency-dependent phenomena. However it is prohibitively expensive to simulate the practical large board cases and the resultant tabulated S-parameter cannot be directly used to quantify the crosstalk level. Heracles integrated a novel hybrid solver techniques with improved speed and accuracy, and developed new crosstalk metrics to quantify the crosstalk level by post-processing S-parameter, and Heracles allows designers to achieve full board crosstalk in a few hours as planned intended with using the tool, which significantly reduces the post-layout review time, allows layout optimization and ensures a timely sign-off.

Heracles Solution

Heracles was the first SI signoff tool for high speed designs, and integrated a novel hybrid full-wave EM solver with the same accuracy order as the conventional 3D solver but an order of magnitude faster speed is developed. The hybrid solver takes advantage of the layered nature of the PCB layout and adopts the idea of layer-by-layer decomposition to reduce the complexity of the problem and achieve the computation speed optimized for full board crosstalk scan. With automated SI signoff flow, we are able to achieve the complete full board crosstalk scan in a few hours as intended with using the tool, which significantly reduces the post-layout check time, allows layout optimization, and ensures the full board coverage.

Key Points

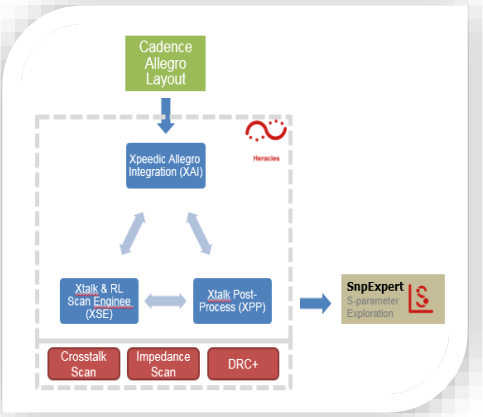
- Heracles provides an automated SI signoff flow for high speed design, and enable quick crosstalk scan, impedance scan and design rule check beyond Allegro.
- Built-in versatile EM solver engines with controllable accuracy and speed to achieve full board scan within a few hours, including FEM3D solver, Hybrid Solver and Pure Via Solver.
- Introduce frequency domain integrated crosstalk noise (ICN) and time domain waveform TDT as crosstalk metrics, and allows quick assessment of the crosstalk by simply comparing them against the pass/warning/failure thresholds.
- Built-in high speed I/O compliance such as Ethernet, PCI Express, DDR, USB, SATA and SAS, which crosstalk poses great challenges for high speed PCB designers with the ever increasing data rate.
- Provides two flexible ways to select crosstalk scan areas with potential SI issues, either by net matching rules defined in high speed I/O compliances or selected manually.
- Heracles XSE provides interactive interface to invoke ViaExpert to visualize, sweep and optimize crosstalk model, and also export to HFSS for better correlation.
- Support intuitive crosstalk level display for the selected nets in either a table or plot format. It also maps to the layout with different colors to allow quick hotspot location identification

FEATURES

Heracles Flow Chart

The crosstalk scan first starts with the signal net scanning based on the user configuration of the high speed interface definition in XAI (Xpeedic Allegro Interface). The selected nets in the via pin field and breakout region under connector or BGA package are automatically extracted without user intervention. Then the hybrid solver managed by XSE is applied to run the full-wave simulation

with proper cut-out of the regions of interest. XPP provides powerful post-processing capability for crosstalk and impedance scan. This flow is automatically repeated for the rest of the high speed nets to achieve the full board crosstalk scan.



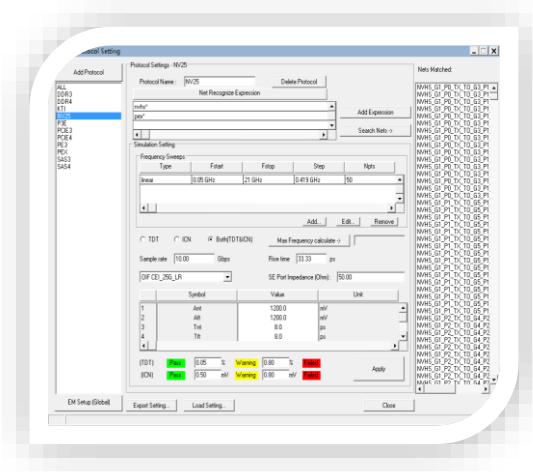
Heracles Flow Chart

XSE with Controllable Accuracy and Speed

Heracles built-in 3 EM solver technologies with controllable accuracy and speed, such as FEM3D, Hybrid Solver and Pure Via Solver. The fast full-board crosstalk analysis is achieve in a few hours as planned by repeatedly scanning the high speed nets defined by the users, which significantly reduces the post-layout check time and ensures signal integrity sign-off.

Easy Protocols Definition

Heracles built-in several crosstalk compliances for high speed I/O interface such as Ethernet, PCI Express, DDR, USB, SATA/SAS, etc. Based on the data rate of those nets recognized by protocols, the frequency range for the simulation is automatically determined though user changeable.

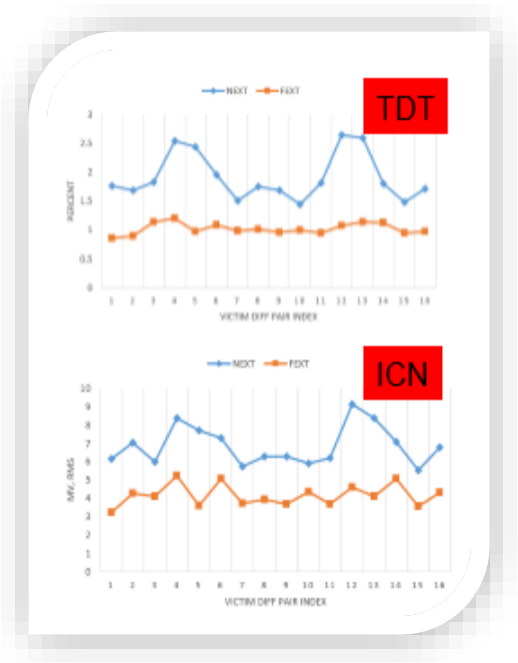


Protocols Definition

Accurate Crosstalk Evaluation

Crosstalk metrics such as frequency domain integrated crosstalk noise (ICN) and time domain waveform TDT are derived from the S-parameter, which allows quick assessment of the crosstalk by simply comparing them against the

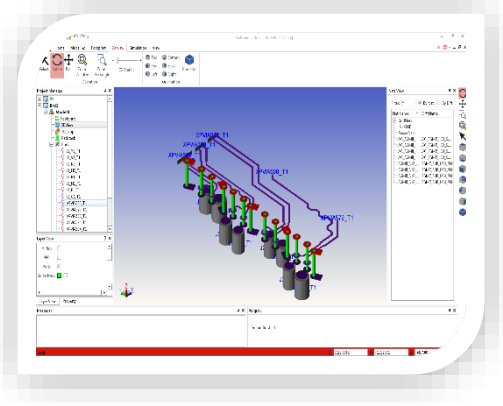
pass/warning/failure thresholds.



Crosstalk Metrics

Intuitive 3D View

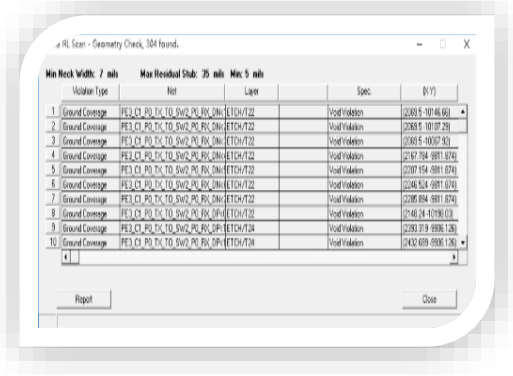
XSE will invoke ViaExpert to display 3D view, sweep and optimize cut-out model from crosstalk hotspot area, and export the simulation project to HFSS for better correlation.



3D View

DRC+ Beyond Allegro

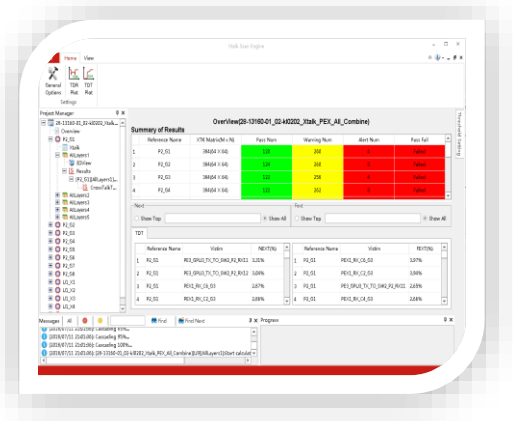
Heracles support multiple geometry check beyond Allegro, including padstack check, backdrill check, ground coverage check and trace necking check.



DRC+

Powerful Post Process

The resultant crosstalk level for the selected nets is shown in either a table or plot format. It also maps to the layout with different colors to allow quick layout location identification. XSE also built-in crosstalk and impedance plot, and invoke SnpExpert to explore more advanced parameters, such as ICN, ILD, COM and so on.



Crosstalk Summary Report

Data Sheet

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