# Robust Amplifiers Provide Integrated Overvoltage Protection

By Eric Modica and Michael Arkin

Faulty performance, or even damage, can occur when an op amp's input voltage exceeds the specified input-voltage range, or—in extreme cases—the amplifier's supply voltage. This article discusses some common causes and effects of *overvoltage conditions*, how cumbersome *overvoltage protection* can be added to an unprotected amplifier, and how the *integrated overvoltage protection* of newer amplifiers provides designers with a compact, robust, transparent, cost-effective solution.

All electronic components have upper limits to the applied voltages they can tolerate. When any of these upper limits are exceeded, the effects can range from momentary interruption of operation to system latch-up to permanent damage. The amount of overvoltage a given component can tolerate depends on several factors, including whether the part is installed or incidentally contacted, the amplitude and duration of the overvoltage event, and the robustness of the device.

Precision amplifiers, often the first component in sensor measurement signal chains, are the most exposed to overvoltage faults. When selecting a precision amplifier, system designers must be aware of the *common-mode input range* of the amplifier. On the data sheet, the common-mode input range may be specified by the *input voltage range* (IVR), or in the test conditions for the *common-mode rejection ratio* (CMRR), or both.

## Real World Causes of Overvoltage Conditions

Amplifiers require: *overvoltage* protection to protect against faults caused by power-supply sequencing, sleep-mode switching, and voltage spikes; and *ESD* protection to protect against faults caused by *electrostatic discharge* (ESD), even during handling. When *installed*, the device can be subjected to system power sequence conditions, which cause repetitive overvoltage stress. System designers seek methods of routing the fault currents away from sensitive components, or limiting those fault currents enough to avoid damage.

In complex *distributed power architecture* (DPA) systems with multiple supply voltages, power-supply sequencing allows the supplies powering various portions of the system circuitry to turn on and off at different times. Improper sequencing can cause overvoltage and latch-up conditions to occur on any pin on any device.

With an increasing focus on energy efficiency, many systems implement complex *sleep* and *standby* modes. This means that some sections of a system may be powered down while others may remain powered and active. As with supply sequencing, these situations can cause unpredictable overvoltage events, but primarily on input pins.

Many types of sensors can generate unexpected output spikes that are unrelated to the physical phenomena they are meant to measure. This type of overvoltage condition generally affects only input pins.

Electrostatic discharge is a well-known overvoltage event that often occurs before the component is installed. The damage it can cause is so prevalent that industry-driven specifications, such as JESD22-A114D, determine how to test and specify the semiconductor's ability to withstand various types of ESD events. Almost all semiconductor products incorporate some form of integrated protection devices. The AN-397 Application Note, "Electrically Induced Damage to Standard Linear Integrated Circuits: The Most Common Causes and the Associated Fixes to Prevent Reccurrence," is a good reference that covers this topic in detail. ESD cells are designed to go into a low-impedance state after a high-energy pulse. This does not limit the input current, but it does provide a low-impedance path to the supply rails.

## A Simple Case Study: Power-Supply Sequencing

As mixed-signal circuits become ubiquitous, so too does the need for multiple supplies on a single PCB. See the AN-932 Application Note, "Power Supply Sequencing," for a look at some subtle issues to consider in new designs, especially when several unrelated power supplies are required.

Precision amplifiers can fall victim to this condition. Figure 1 shows an op amp configured as a differential amplifier. The amplifier senses the current through $R_{SENSE}$ and provides an output proportional to the resultant voltage drop. Care must be taken that the divider formed by $R_3$ and $R_4$ biases the inputs somewhere within the specified IVR. If the amplifier's supply voltage is not derived from $V_{SY}$, and $V_{CC}$ comes up after $V_{SY}$, the voltage at the inverting input of A1 will be:

$$V_- = V_{SY} - (I_- \times R_1) \quad (1)$$

where $I_-$ depends on the input impedance of A1 with no supply. If the amplifier is not designed to handle overvoltage conditions, the most likely current path will be through an ESD diode, clamp diode, or parasitic diode to the power supply or ground. Damage can occur if this voltage falls outside of the IVR or if the current exceeds the data sheet maximum rating.

The ESD structures used on overvoltage-protected amplifiers, such as the ADA4091 and ADA4096, are not diodes, but DIAC (bidirectional "diode for alternating current") devices, making these amplifiers tolerant of overvoltage conditions, even without power.
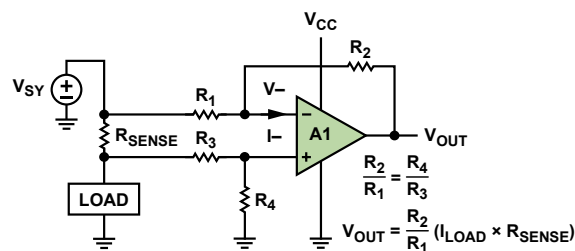


Figure 1. Differential amplifier high-side current sensor. If $V_{SY}$ powers up before $V_{CC}$, the amplifier's input voltage or current can exceed the data sheet maximum.

## Fault Conditions in Operational Amplifiers

Figure 2 shows an N-channel JFET input stage ($J_1$, $J_2$, $R_1$, and $R_2$), followed by a secondary gain stage and output buffer (A1). When the open-loop amplifier is within its specified IVR, the differential input signal ($V_{IN+} - V_{IN-}$) is 180 degrees out of phase with $V_{DIFF}$. When connected as a unity-gain buffer, as shown, if the common-mode voltage at $V_{IN+}$ exceeds the amplifier's IVR, $J_1$'s gate-drain will un-pinch and conduct the entire 200-µA stage current. As long as J1's gate-drain voltage remains reverse-biased, a further increase at $V_{IN+}$ causes no change in $V_{DIFF}$ ($V_{OUT}$ stays at the positive rail). Once $J_1$'s gate-drain becomes forward-biased, however, a further increase in $V_{IN+}$ *raises* the voltage at A1's inverting input, causing an undesirable phase-reversal between the input signal and $V_{DIFF}$.
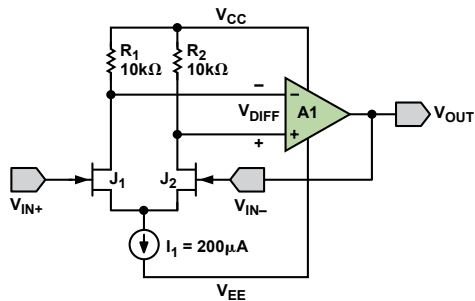
Figure 2. A conceptual N-channel, JFET-input op amp.

Figure 3 shows an example of phase reversal at the output of A1. Unlike bipolar input amplifiers, JFET amplifiers are prone to phase reversal because their inputs are not clamped. CMOS amplifiers are typically immune to phase reversal because the gates are electrically isolated from the drains. If phase inversion doesn't occur, op amp manufacturers will often state this on the data sheet. Phase inversion is possible if: the amplifier inputs are not CMOS, the maximum differential input is $V_{SY}$, and the data sheet does not claim immunity to phase inversion. Although phase inversion by itself is nondestructive, it can cause positive feedback, which leads to instability in servo loops.
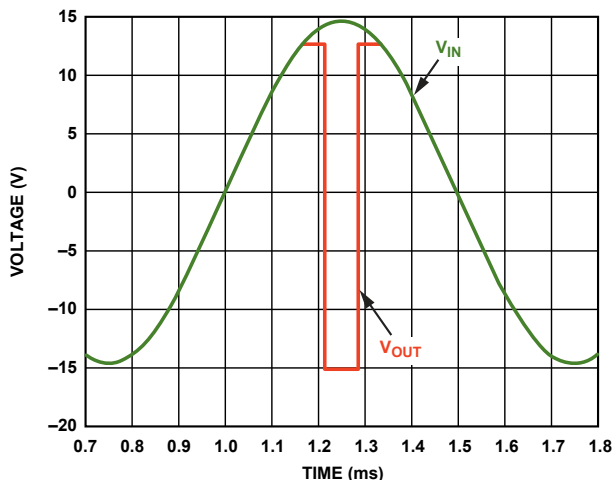


Figure 3. When $V_{IN}$ exceeds the specified IVR, input phase inversion causes the output of the amplifier to become negative.

System designers also have to be concerned about what happens when the amplifier inputs are pulled outside the power supplies. Most often this fault condition occurs when power-supply sequencing causes a source signal to be active before the amplifier supplies turn on, or when a power supply spikes during turn-on, turn-off, or in operation. This condition is destructive for most amplifiers, especially if the overvoltage is greater than a diode drop.

Figure 4 shows a typical bipolar input stage with ESD protection diodes and clamp diodes. In a buffer configuration, when $V_{IN+}$ exceeds either rail, ESD and clamp diodes will be forward biased. With very low source impedance, these diodes will conduct as much current as the source will allow. Precision amplifiers, such as the AD8622, provide a modicum of differential protection by including 500-$\Omega$ resistors in series with the inputs to limit the input current when a differential voltage is applied, but they protect only as long as the maximum input current specification isn't exceeded. If the maximum input current is 5 mA, then the maximum allowed differential voltage is 5 V. Note that these resistors are not in series with the ESD diodes, so they cannot limit current to the rails (for example, during an overvoltage condition).
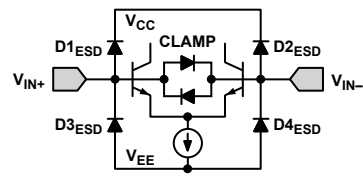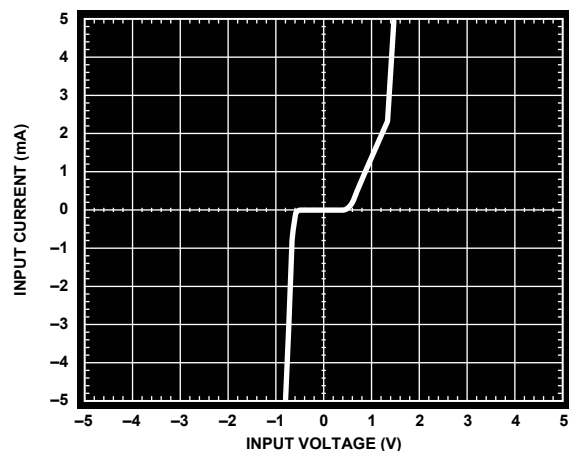


Figure 4. A bipolar input stage showing ESD, and differential protection diodes.

Figure 5 shows the input current-voltage relationship of an unprotected bipolar op amp with differential input and overvoltage applied simultaneously. Once the applied voltage exceeds a diode drop, the current can become destructive, degrading or even destroying the op amp.
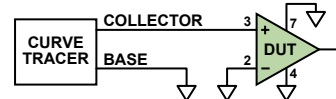


Figure 5. Op amp input current as the differential input voltage exceeds a diode drop.

### External Input Overvoltage Protection

From the earliest days of semiconductor op amps, IC designers have had to deal with trade-offs between chip architecture and the external circuitry needed to deal with its weaknesses. Fault protection has been among the most difficult of problem areas (for examples, see MT-036, "Op Amp Output Phase-Reversal and Input Over-Voltage Protection" and MT-069, "In-Amp Input Overvoltage Protection").

Two properties system designers need precision op amps for are their low offset voltage ($V_{OS}$) and high common-mode rejection ratio (CMRR), both of which simplify calibration and minimize dynamic error. To maintain these specifications in the presence of electrical overstress (EOS), bipolar op amps often include internal clamp diodes and small limiting resistors in series with their inputs, but these cannot address fault conditions caused when the inputs exceed the rails. To add protection, the system designer can implement circuitry such as that shown in Figure 6.
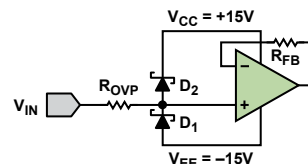


Figure 6. Precision op amp with external protection using a current-limiting resistor and two Schottky diodes. $R_{FB}$ is set equal to $R_{OVP}$ to balance offsets due to input bias currents.

$R_{OVP}$ will limit the current into the op amp if the signal source at $V_{IN}$ powers up first. Schottky diodes have a forward voltage 200 mV less than typical small-signal diodes, so all of the overvoltage current will be shunted through external diodes $D_1$ and $D_2$. However, these diodes can degrade the op amp specifications. For example, the reverse leakage plots from the 1N5711 (see Figure 7) can be used to determine the CMRR penalty for a given OVP resistor. The reverse leakage of the 1N5711 is 0 nA at 0 V and 60 nA at 30 V. With a common mode of 0 V, the additional $I_{OS}$ caused by $D_1$ and $D_2$ depends on how well their leakages match. When $V_{IN}$ is taken to +15 V, $D_1$ will be reverse biased by 30 V, and $D_2$ will have 0 V bias. Thus, an additional 60 nA flows into $R_{OVP}$. When the input is taken to –15 V, $D_1$ and $D_2$ swap positions electrically, and 60 nA flows out of $R_{OVP}$. The additional $I_{OS}$ caused by the protection diodes at any common mode is simply:

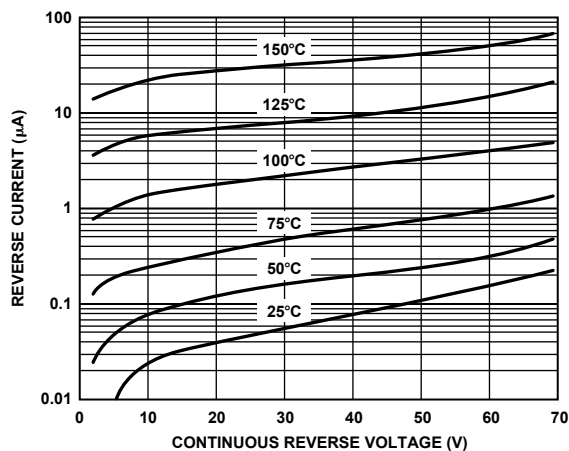$$I_{OSaddr} = I_{D1} - I_{D2} \qquad (2)$$



Figure 7. 1N5711 reverse current vs. continuous reverse voltage.

From Equation 2, the $V_{OS}$ penalty can be derived at the extremes of the common-mode range as follows:

$$V_{OSpenalty} = I_{OSaddr} \times R_{OVP} \qquad (3)$$

Using 60 nA as the leakage of the 1N5711 at 30 V, and a 5-k$\Omega$ protection resistor, $V_{OS}$ at each extreme would be increased by 300 µV, causing an additional 600 µV $\Delta V_{OS}$ over the entire input-voltage range. In data sheet terms, an op amp with 110-dB CMRR would suffer a 17-dB reduction. Inserting a feedback resistor to equalize source impedance only helps when the common mode is 0 V, and does nothing to prevent additional $I_{OS}$ over the full common-mode range. Table 1 shows the same calculation for diodes commonly used for protecting precision amplifiers. For CMRR penalty calculations, a 5-k$\Omega$ protection resistor is assumed. All costs are recent quotes (2011) in USD from www.mouser.com.

Another possible drawback to the method shown in Figure 6 is that the protection diodes shunt the overvoltage current into the supplies. If, for example, the positive supply cannot sink a significant amount of current, the overvoltage current can force the positive supply voltage to increase.

One way to prevent this is to use back-to-back Zener diodes from the positive input to ground, as shown in Figure 8. When the Zener voltage of either $D_1$ or $D_2$ is exceeded, the diode shunts the overvoltage current to ground, protecting the power supplies. This configuration prevents charge pumping during overvoltage conditions, but Zener diodes have higher leakage current and capacitance than small-signal diodes. In addition, Zener diodes have a soft-knee characteristic in their leakage current profile. This, as described previously, adds an additional CMRR penalty over the amplifier's common-mode range. For example, the BZB84-C24 is a back-to-back Zener diode pair with a working voltage between 22.8 V and 25.6 V. The reverse current is specified as 50 nA max at 16.8 V, but the manufacturer doesn't specify what the leakage is closer to the Zener voltage. Also, to achieve a sharper breakdown characteristic, Zener diodes are generally made of more highly doped diffusions than their small-signal cousins. This causes a relative increase in parasitic capacitance, which translates to increased distortion (especially at higher amplitudes) and increased instability.
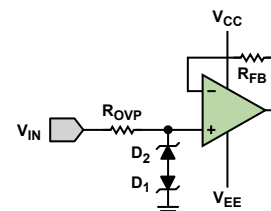


Figure 8. Precision op amp with external protection using a current-limiting resistor and two Zener diodes.

### Early Integrated Overvoltage Protection

The previous section discussed drawbacks to some commonly used methods of external amplifier protection. Some of these drawbacks could be avoided if the amplifier itself is designed to tolerate a large input overvoltage. Figure 9 shows a common integrated protection scheme used on a differential input pair.
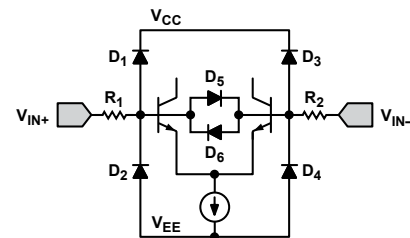


Figure 9. A differential input pair with resistive overvoltage protection (ESD protection not shown).

This circuit includes input protection resistors on both amplifier inputs. Although overvoltage protection is generally needed on only one input, equalizing the parasitic capacitance and leakage

**Table 1. Commonly Used Protection Diodes and Their Impact on a 110-dB CMRR Precision Op Amp**

|  | 1N5711 | BAV99 | PAD5 | BAS70-04 | 1N914 | BZB84-C24 |
|---|---|---|---|---|---|---|
| $I_{OSaddr}$ (nA) | 60 | 10 | <<0.005 | 8 | 40 | 50 |
| $V_{OSpenalty}$ (µV) | 600 | 100 | 0 | 80 | 400 | 500 |
| CMRR Penalty (dB) | 17 | 6 | 0 | 5 | 14 | 16 |
| Cost @ 1k Quantities | $0.07 | $0.015 | $3.52 | $0.095 | $0.01 | $0.034 |

at each input reduces distortion and offset current. Furthermore, the diodes do not have to handle ESD events, so they can be relatively small.

Adding resistance, either external or internal, adds to the amplifier's root-sum-square (RSS) thermal noise (Equation 4):

$$E_{n,total} = \sqrt{(e_{n,op\ amp})^2 + (e_{n,Rovp})^2 + (R_S \times i_{n,op\ amp})^2} \quad (4)$$

If a 1-kΩ resistor is used to protect an op amp with 4-nV/√Hz of noise, the total voltage noise will increase by √2. Integrating the protection resistors doesn't change the fact that overvoltage protection increases the input-referred voltage noise, but integrating $R_1$ and $R_2$ with the op amp ensures that the data sheet noise specification covers the protective circuitry.

To avoid the noise-overvoltage trade-off requires a protective circuit that presents a low resistance when the amplifier inputs are within the specified range and a very high resistance when the amplifier inputs exceed the rails. This characteristic would provide improved overvoltage protection on-demand, thus lowering the overall noise contribution under normal operating conditions. Figure 10 shows one circuit implementation that behaves in this way.
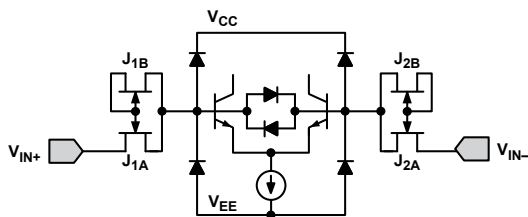


Figure 10. Input differential pair with active overvoltage protection.

$\mathcal{J}_{xy}$ are all P-channel JFETs; they are depletion mode devices, so the channel is the same polarity as the source and drain. When the amplifier input levels are between the rails, $J_{1A}$ and $J_{2A}$ act as simple resistors with resistance equal to $R_{DSON}$ because the input bias currents are small enough that any potential difference between the channel and gate won't pinch the channel closed. If $V_{IN+}$ were to exceed the negative supply by a diode drop, current would begin to flow through $J_{1A}$, causing the drain to pinch closed. This transition is actually $J_{1A}$ moving out of triode and into the linear region. If $V_{IN+}$ were to exceed the positive supply voltage by a diode drop, $J_{1A}$ would act as a lateral PNP. $V_{IN+}$ to the gate would act as a forward-biased emitter-base junction, with the other junction acting as the base-collector, standing off overvoltage.

The current-voltage plot of Figure 11 shows the change in input impedance of a FET-protected op amp when subjected to an overvoltage sweep. The $R_{DSON}$ of the protection FET is 4.5 kΩ; as the amplifier's positive input is pulled above the rail, the protection FET's resistance increases rapidly to 22 kΩ at 30 V, limiting the input current to 1.5 mA.
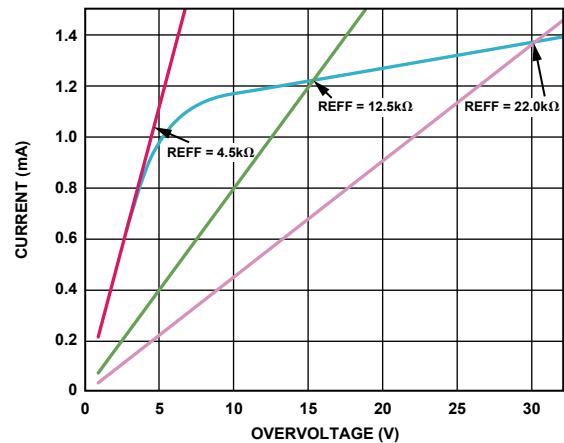


Figure 11. Effective input impedance of a FET protected op amp when subjected to a dc overvoltage sweep.

### The Benefits of Integration

Amplifiers such as the ADA4091 and ADA4096 demonstrate that robust, overvoltage-tolerant op amp inputs can be achieved with a minimal impact on precision (as in Figure 10). The ADA4096 provides 32-V protection, regardless of supply levels—eliminating the need for external components that can either be inexpensive but vastly degrade the amplifier's precision, or precise but more costly than the amplifiers themselves.

Figure 12 shows the ADA4096-2 in a 2-mm × 2-mm LFCSP package next to a couple of discrete components often used for external input protection. The ADA4096-2's integrated protection provides a significantly reduced PCB footprint; its effects are included in the op amp's specifications; and it protects the amplifier even when power is not applied (see Figure 13). In addition, the ADA4091 and ADA4096 have rail-to-rail inputs and outputs (RRIO) and are free from phase-inversion over the entire overvoltage protection range (see Figure 14). These benefits allow system designers to worry a little less about power-supply sequencing and latch-up.
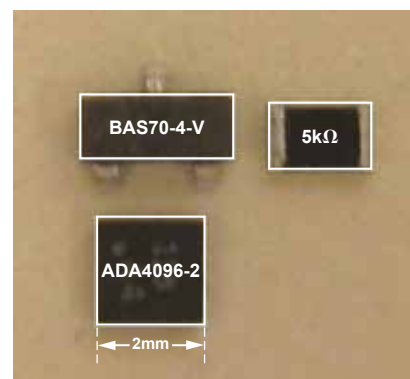


Figure 12. The ADA4096-2 in a 2-mm × 2-mm package occupies less space than two components commonly used for external voltage protection.
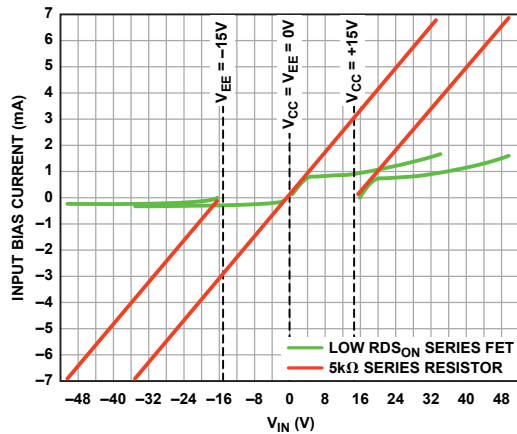
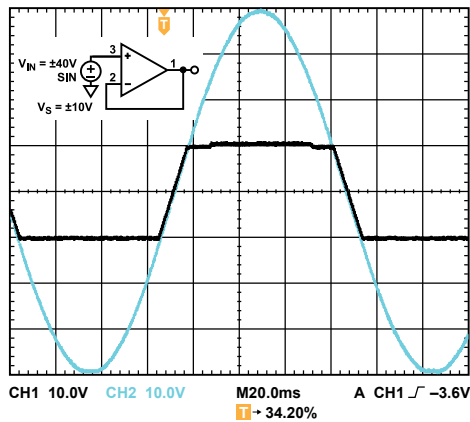Figure 13. ADA4096-2 input OVP current limiting with and without power.



Figure 14. ADA4096-2 on ±10-V supplies with the inputs pulled 30 V above and below the rails.

## Conclusions

In summary, integrated overvoltage protection provides many benefits:

1. Improved robustness and precision in analog signal chains.
2. Reduced time-to-market (TTM), shorter design time, and reduced testing requirements.
3. Reduced bill of materials (BOM) cost.
4. Fewer components required in approved component lists.
5. Reduced PCB footprint/higher density.
6. Lower failure rates.

## References

1N914 data sheet available at www.fairchildsemi.com.

1N5711 data sheet available at www.st.com.

BAV99, BAS70-04, and BZB84-C24 data sheets available at www.nxp.com.

PAD5 data sheet available at www.vishay.com.

JESD22-A114D standard available at www.jedec.org.

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