

# Intel<sup>®</sup> Quark SoC X1000

Platform Design Guide (PDG)

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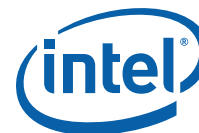
## Contents

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<b>1.0</b>	<b>Introduction</b>	17
1.1	Terminology	18
<b>2.0</b>	<b>Stack-Up and PCB Considerations</b>	19
2.1	Printed Circuit Board (PCB) Considerations	19
2.2	Low Halogen Flame Retardant Stack-Up Considerations	21
2.2.1	Low Halogen Background	21
2.2.2	Choosing a Low Halogen Material	21
2.2.3	Electrical Limits of Low Halogen Material Properties	21
2.3	Reference Planes	22
2.4	Backward and Forward Coupling Coefficient Calculation	22
2.5	Single-Ended and Differential-Impedance Transmission Line Specifications	24
2.6	Minimizing the Effect of Fiber Weave	25
2.6.1	Overview of Fiber Weave	25
2.6.2	Fiber Weave Effect versus Transfer Rate and Trace Length	27
2.6.3	Specific Routing Configurations	28
2.6.4	Offset Routing	28
2.6.5	Zig-Zag or Slanted Routing	28
2.6.6	Image Rotation	29
2.6.7	Using Alternate PCB Materials	30
<b>3.0</b>	<b>DDR3 Memory Design Guidelines</b>	31
3.1	Memory General Introduction	31
3.1.1	Supported Memory Configurations	31
3.1.2	Memory Population Rules	31
3.1.3	Reference Documents	31
3.1.4	Design Constraints-based Routing	31
3.2	Memory Signal Description	32
3.3	Memory Topology Guidelines	32
3.3.1	Single Rank Fly-by Topology with Active VTT Termination	33
3.3.2	Memory Stackup Guidelines	38
3.3.3	Memory Configurations and Connectivity	39
3.3.3.1	ODT Signal Connectivity and Support	39
3.3.4	Memory Physical Layout Guidelines	39
3.3.4.1	General Routing Guidelines	39
3.3.4.2	Byte Lane Placement	39
3.3.4.3	Via Stitching and Placement	40
3.3.5	Memory Bit and Byte Lane Swapping	40
3.3.6	Memory Length Matching Guidelines	40
3.3.6.1	Length Matching and Length Formulas	40
3.3.6.2	Package Length Compensation	40
3.3.7	Memory Decoupling Guidelines	40
3.4	Memory Reference Voltage and Compensation Guidelines	40
3.4.1	SoC DDR Reference Voltage	40
3.4.2	DRAM Reference Voltage	41
3.4.3	DRAM ZQ Calibration	41
3.4.4	Routing Guidelines for Compensation Signals	41
3.5	DataMask Guidelines	41
<b>4.0</b>	<b>PCI Express* Design Guidelines</b>	43
4.1	PCIe* General Introduction	43
4.1.1	Description	43
4.1.2	Supported Configuration Options for PCIe* Ports	43



- 4.1.3 PCI Express\* Lane Polarity Inversion.....43
- 4.1.4 PCI Express\* Port Lane Reversal.....44
- 4.1.5 PCIe\* Port Disabling Guidelines.....44
- 4.1.6 Length Matching Guidelines.....44
- 4.1.7 Difference Between PCIe Ports and Lanes.....44
- 4.1.8 Impedance Compensation and Voltage Reference.....45
- 4.1.9 Reference Documents.....45
- 4.2 PCIe\* Signal Descriptions .....45
  - 4.2.1 Signal Groups .....45
- 4.3 PCIe\* Topology Guidelines .....46
  - 4.3.1 Expansion Card Connector Topology.....46
- 5.0 Universal Serial Bus 2.0 Design Guidelines.....51**
  - 5.1 USB 2.0 General Introduction .....51
    - 5.1.1 Description .....51
    - 5.1.2 Compliance Documents .....51
  - 5.2 USB 2.0 Signal Descriptions .....52
    - 5.2.1 Signal Groups .....52
    - 5.2.2 Overcurrent Protection .....52
  - 5.3 USB 2.0 Topology Guidelines.....53
    - 5.3.1 External Topologies.....53
    - 5.3.2 USB Connector Recommendations.....56
      - 5.3.2.1 External Connector Recommendations.....56
    - 5.3.3 Daughter Card .....57
      - 5.3.3.1 Daughter Card Design Guidelines .....58
  - 5.4 USB 2.0 Stackup Guidelines .....58
    - 5.4.1 Stackup and Layer Utilization Guidelines .....58
  - 5.5 USB 2.0 Configuration, Connectivity, Block Diagram .....58
    - 5.5.1 Port Power Delivery.....58
  - 5.6 USB 2.0 Length Matching Guidelines .....59
    - 5.6.1 Length Matching and Length Formulas .....59
  - 5.7 USB 2.0 Additional Guidelines.....59
    - 5.7.1 EMI and ESD Protection .....59
  - 5.8 USB 2.0 Disabling and Termination Guidelines .....59
- 6.0 I2C\* Interface Design Guidelines.....61**
  - 6.1 I2C\* General Introduction.....61
    - 6.1.1 Description .....61
    - 6.1.2 Reference Specifications .....61
  - 6.2 I2C\* Signal Descriptions.....61
    - 6.2.1 Signal Groups .....61
  - 6.3 I2C\* Topology Guidelines .....62
    - 6.3.1 General Design Considerations .....62
    - 6.3.2 Detailed Routing Requirements.....62
  - 6.4 I2C\* Connectivity .....63
  - 6.5 I2C\* Additional Guidelines .....64
  - 6.6 Terminating Unused I<sup>2</sup>C Signals.....64
- 7.0 SDIO Interface Design Guidelines .....65**
  - 7.1 SDIO General Introduction.....65
    - 7.1.1 Description .....65
  - 7.2 SDIO Signal Descriptions .....65
    - 7.2.1 Signal Groups .....65
  - 7.3 SDIO Topology Guidelines.....66
  - 7.4 Terminating Unused SDIO Signals.....66
- 8.0 UART Interface Design Guidelines.....69**



- 8.1 General Introduction..... 69
  - 8.1.1 Description..... 69
- 8.2 General Purpose Signal Descriptions ..... 69
  - 8.2.1 Signal Groups ..... 69
- 8.3 UART Topology Guidelines ..... 69
- 8.4 Additional Guidelines ..... 70
- 8.5 Terminating Unused UART Signals ..... 70
- 9.0 General Purpose SPI Interface Design Guidelines ..... 73**
  - 9.1 General Introduction..... 73
    - 9.1.1 Description..... 73
  - 9.2 General Purpose Signal Descriptions ..... 73
    - 9.2.1 Signal Groups ..... 73
  - 9.3 Topology Guidelines..... 74
  - 9.4 Terminating Unused SPI Signals ..... 77
- 10.0 Platform Clocks Design Guidelines ..... 79**
  - 10.1 Platform Clock General Introduction..... 79
    - 10.1.1 Description..... 79
  - 10.2 Platform Reference Clock Signal Descriptions ..... 80
  - 10.3 Platform Clocks Topology Guidelines ..... 81
    - 10.3.1 Differential Clock Routing Topology..... 81
      - 10.3.1.1 Differential Routing Considerations ..... 82
      - 10.3.1.2 Stitching Via Usage and Placement..... 82
    - 10.3.2 Single Ended Clock Routing Topology ..... 82
  - 10.4 25 MHz Crystal and Associated RC Components..... 83
    - 10.4.1 Crystal External Load Capacitor Requirements..... 84
    - 10.4.2 25 MHz Crystal Routing Considerations..... 85
- 11.0 SPI Flash Design Guidelines ..... 87**
  - 11.1 Serial Peripheral Interface (SPI) General Introduction ..... 87
    - 11.1.1 Description..... 87
  - 11.2 Serial Peripheral Interface (SPI) Signal Description ..... 87
  - 11.3 Serial Peripheral Interface (SPI) Topology Guidelines ..... 88
    - 11.3.1 SPI Single Flash Device Topology Guidelines ..... 88
      - 11.3.1.1 SPI Single Flash Device Routing Guideline ..... 88
      - 11.3.1.2 SPI Single Flash Device Length Matching Requirement ..... 89
    - 11.3.2 Dual SPI Devices + Bootflash Topology Guidelines ..... 90
      - 11.3.2.1 Multiple SPI Flash Device + Bootflash Routing Guideline..... 90
      - 11.3.2.2 Dual SPI Flash Device Routing Guideline ..... 91
    - 11.3.3 Boot BIOS Destination ..... 91
  - 11.4 Serial Flash Vendors ..... 91
- 12.0 RTC Design Guidelines ..... 93**
  - 12.1 Real Time Clock General Introduction..... 93
    - 12.1.1 Description..... 93
  - 12.2 Real Time Clock Signal Descriptions ..... 93
    - 12.2.1 Signal Groups ..... 93
    - 12.2.2 State Power Good Indicators..... 94
  - 12.3 Real Time Clock Topology Guidelines..... 95
    - 12.3.1 RTC External Example Circuit..... 95
    - 12.3.2 General RTC Layout Considerations..... 96
    - 12.3.3 External Capacitors ..... 96
  - 12.4 RTC External Battery Connection ..... 97
    - 12.4.1 RTC Holdup Calculation ..... 98
  - 12.5 RTC External RTCRST# Circuit ..... 99
  - 12.6 RTC-Well Input Strap Requirements..... 100



- 13.0 Asynchronous Signals Design Guidelines** ..... 101
  - 13.1 Asynchronous Signals General Introduction ..... 101
    - 13.1.1 Description ..... 101
  - 13.2 Asynchronous Signal Descriptions ..... 101
    - 13.2.1 Signal Groups ..... 101
  - 13.3 Asynchronous Signals Topology Guidelines ..... 101
  - 13.4 General GPIO Topology Guidelines ..... 102
- 14.0 Platform Power Delivery Requirements** ..... 105
- 15.0 Platform Reset Considerations** ..... 109
  - 15.1 Platform Reset General Introduction ..... 109
    - 15.1.1 Description ..... 109
  - 15.2 Signal Description ..... 109
    - 15.2.1 Signal Groups ..... 109
  - 15.3 Additional Guidelines ..... 110
    - 15.3.1 PMC\_V3P3\_S0\_EN# Usage Model ..... 110
    - 15.3.2 PMC\_V1P5\_S0\_EN# Usage Model ..... 110
    - 15.3.3 PMC\_V1P0\_S0\_EN# Usage Model ..... 110
    - 15.3.4 PMC\_V3P3\_S3\_EN# Usage Model ..... 110
    - 15.3.5 PMC\_V1P5\_S3\_EN# Usage Model ..... 110
    - 15.3.6 PWRBTN# Usage Model ..... 110
    - 15.3.7 RSTBTN# Usage Model ..... 110
    - 15.3.8 Power-well Isolation Control Signal Requirements ..... 111
    - 15.3.9 platform\_s5\_pwrok Generation ..... 111
    - 15.3.10 platform\_S3\_pwrok Generation ..... 111
    - 15.3.11 platform\_S0\_1P0\_pwrok Generation ..... 111
    - 15.3.12 platform\_S0\_1P5\_pwrok Generation ..... 111
    - 15.3.13 Glue Logic Device ..... 111
    - 15.3.14 Additional Power Sequencing Considerations ..... 112
    - 15.3.15 Power Sequence Timing Diagram ..... 112
- 16.0 Critical Low Speed Signals Design Guidelines** ..... 113
  - 16.1 Critical Low Speed Signals General Introduction ..... 113
    - 16.1.1 Description ..... 113
  - 16.2 Critical Low Speed Signal Descriptions ..... 113
    - 16.2.1 Signals Group ..... 113
  - 16.3 Additional Guidelines ..... 114
- 17.0 Electromagnetic Interference** ..... 115
  - 17.1 Electromagnetic Interference (EMI) General Introduction ..... 115
    - 17.1.1 Description ..... 115
  - 17.2 Exercising the System for EMC Testing ..... 115
  - 17.3 EMI Source ..... 117
    - 17.3.1 Current Loop Radiation ..... 117
    - 17.3.2 Voltage Regulator Module Current Loop Radiation ..... 118
    - 17.3.3 Common Mode Radiation ..... 120
  - 17.4 EMI Optimization Guideline ..... 121
    - 17.4.1 Avoid Changing Referencing, Lack of Referencing, Void-crossing, and Split-crossing ..... 121
    - 17.4.2 Avoid Signal Traces Too Close to the Edges of Planes ..... 122
    - 17.4.3 Avoid Unnecessary Traces Too Close to IO and Other Connectors ..... 122
    - 17.4.4 EMI Mitigation through Stitching and Decoupling Capacitors ..... 123
      - 17.4.4.1 Stitching Capacitors ..... 124
      - 17.4.4.2 Decoupling Capacitors ..... 126
    - 17.4.5 Common Mode Filter ..... 128
      - 17.4.5.1 USB Common Mode Choke Recommendation ..... 128



17.4.6	USB 2.0 Common Mode Chokes .....	128
17.4.7	Spread Spectrum Clocking .....	129
17.4.8	Signal Scrambling .....	130
17.4.9	Memory Down .....	131
17.4.9.1	Layer Transition.....	131
17.4.9.2	Clustered Signal Vias.....	131
17.4.10	Cable/Adaptor Shielding .....	132
17.5	Design Checklist Items.....	133
<b>18.0</b>	<b>Electrostatic Discharge (ESD)</b> .....	<b>135</b>
18.1	Electrostatic Discharge (ESD) General Introduction .....	135
18.1.1	Description.....	135
18.1.2	Reference Specifications.....	136
18.2	ESD Protection.....	136
18.2.1	ESD Ground-Fill .....	137
18.2.2	Ground-Fill Background.....	137
18.2.3	USB ESD Diode Recommendation .....	138
18.2.4	Series RC Filters.....	138
18.2.5	Sensitive Nets.....	141
18.3	USB ESD Component Selection Guidelines .....	142
18.3.1	USB 2.0 ESD Protection.....	142
18.3.2	USB 2.0 ESD Protection Diode Vendors .....	144
18.4	Design Checklist Items.....	146
<b>19.0</b>	<b>Platform Debug and Test Hooks</b> .....	<b>147</b>
19.1	Platform Debug and Test Hooks General Introduction .....	147
19.1.1	Description.....	147
19.2	Platform Debug Port .....	147
19.2.1	Signal Routing Guidelines .....	147
19.3	JTAG Boundary Scan.....	147
19.3.1	Terminating Unused JTAG Signals.....	147
19.4	Additional Debug Support Guidelines.....	148
19.4.1	Test Points Requirements .....	148
<b>20.0</b>	<b>Design for Testability (DFT)</b> .....	<b>149</b>
20.1	DFT General Introduction .....	149
20.1.1	Description.....	149
20.1.2	Reference Documents .....	149
20.2	DFT Configuration, Connectivity, Block Diagram .....	149
<b>21.0</b>	<b>LAN Design Considerations and Guidelines</b> .....	<b>153</b>
21.1	PHY Overview .....	154
21.1.1	PHY Interconnects .....	154
21.1.2	RMII Interface .....	155
21.1.2.1	RMII Interface Signals .....	155
21.1.2.2	RMII Reference Clock .....	155
21.1.3	MDIO Interface .....	155
21.1.3.1	MDIO Connectivity .....	155
21.2	Platform LAN Design Guidelines.....	155
21.2.1	General Design Considerations for PHYs .....	155
21.2.1.1	Clock Source .....	156
21.2.1.2	Magnetics Module .....	156
21.2.1.3	Criteria for Integrated Magnetics Electrical Qualification .....	156
21.2.2	NVM Configuration for PHY Implementations .....	157
21.2.3	LED Example .....	157
21.2.3.1	RBIAS .....	158
21.3	Intel® Quark SoC X1000 – MDIO/RMII LOM Design Guidelines .....	159



- 21.4 General Layout Guidelines..... 160
- 21.5 Layout Considerations ..... 160
- 21.6 Guidelines for Component Placement..... 160
  - 21.6.1 PHY Placement Recommendations..... 160
- 21.7 MDI Differential-Pair Trace Routing for LAN Design..... 162
- 21.8 Signal Trace Geometry ..... 162
- 21.9 Trace Length and Symmetry ..... 165
- 21.10 Impedance Discontinuities ..... 166
- 21.11 Reducing Circuit Inductance ..... 166
- 21.12 Signal Isolation ..... 166
- 21.13 Power and Ground Planes ..... 166
- 21.14 Traces for Decoupling Capacitors ..... 169
- 21.15 Ground Planes under a Magnetics Module..... 169
- 21.16 Light Emitting Diodes ..... 171
- 21.17 Considerations for Layout ..... 171
- 21.18 Vibrational Mode..... 171
- 21.19 Nominal Frequency ..... 171
- 21.20 Frequency Tolerance ..... 171
- 21.21 Troubleshooting Common Physical Layout Issues ..... 171
- 21.22 Power Delivery ..... 173
- 21.23 Routing Guidelines..... 173
- 22.0 Wireless Modules and Antenna Design Guidelines ..... 175**
  - 22.1 Introduction..... 175
  - 22.2 WLAN System Integration Considerations..... 175
    - 22.2.1 Antenna Integration into the Platform..... 175
    - 22.2.2 Antenna Coexistence..... 176
    - 22.2.3 WiFi Module ..... 176
    - 22.2.4 WiFi Module Connector Types ..... 177
    - 22.2.5 WiFi Antenna Placement ..... 177
    - 22.2.6 Antenna Placement ..... 177
    - 22.2.7 Antenna Cabling ..... 178
    - 22.2.8 Platform Noise Mitigation ..... 178
    - 22.2.9 Antenna Material Choices..... 178
  - 22.3 ZigBee System Integration Considerations ..... 178
    - 22.3.1 ZigBee Antenna Placement..... 178
- A General Differential Signals Design Guidelines ..... 179**
  - A.1 Introduction..... 179
  - A.2 General Differential Routing Guidelines ..... 179
  - A.3 General Differential Length Matching Guidelines ..... 179
    - A.3.1 Length Matching and Length Formulas ..... 179
  - A.4 General Differential Stackup Guidelines..... 182
    - A.4.1 Stackup and Layer Utilization Guidelines ..... 182
  - A.5 General Differential Optimization Guidelines ..... 184
    - A.5.1 Breakout Example and Guidelines ..... 184
    - A.5.2 Via Placement and Via Usage Optimization ..... 185
    - A.5.3 Bend Optimization Guidelines ..... 187
  - A.6 General Differential Reference Planes Guidelines ..... 188
  - A.7 General Docking Connector Recommendations for Differential Interfaces..... 189
- B Exposed Pad\* (e-Pad\*) Design and SMT Assembly Guide..... 191**
  - B.1 Overview ..... 191
  - B.2 PCB Design Requirements ..... 191
  - B.3 Board Mounting Guidelines..... 193
  - B.4 Stencil Design ..... 193

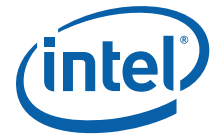


B.5	Assembly Process Flow.....	194
B.6	Reflow Guidelines.....	195



## Figures

1	Intel® Quark SoC X1000 Block Diagram .....	18
2	Single-Ended Microstrip Diagram .....	20
3	Differential-Microstrip Diagram .....	20
4	Backward Coupling Coefficient.....	23
5	Forward Coupling Coefficient.....	23
6	Single-ended Kb Diagram .....	24
7	Differential Kb Diagram .....	24
8	Common Glass Cloths Used in PCB Manufacture .....	26
9	Inhomogeneous Nature of a PCB as Shown in this Cross-Section.....	26
10	Effect of Skew on Differential and Common Mode Signals.....	27
11	Cross-Section of PCB Indicating Effect of PCB Fiber Weave.....	27
12	An Example of Offset Routing.....	28
13	An Example of Zig-Zag Routing .....	29
14	An Example of Slanted Routing.....	29
15	An Example of a PCB Cut Such That Its Edges are Rotated Relative to the Fiber Weave Pattern .....	30
16	DQ/DM - Data Routing Topology for a Single Rank 4L Fly-by Design - PCB Type 3 .....	33
17	DQS - Data Strobes Routing Topology for a Single Rank 4L Fly-by Design - PCB Type 3 .....	33
18	ODT/CKE/CS - Control Routing Topology for a Single Rank 4L Fly-by Design - PCB Type 3.....	35
19	MA/BS/CAS/RAS/ WE - Command Routing Topology for a Single Rank 4L Fly-by Design - PCB Type 3.....	36
20	Clock Routing Topology for a Single Rank 4L Fly-by Design - PCB Type 3 .....	37
21	DDR3 Memory Down Block Diagram.....	39
22	Polarity Inversion on a TX to RX Interconnect.....	44
23	PCI Express* Expansion Card Connector Topology .....	46
24	USB Port Mapping.....	51
25	Sample Over Current Protection Circuit.....	53
26	USB 2.0 MicroUSB Topology.....	53
27	USB 2.0 Mini PCIe Topology .....	55
28	Example of Internal Connector Pin Assignment and Description.....	57
29	Daughter Card .....	58
30	Example of Devices on I2C* Bus.....	63
31	SDIO Topology with Connector .....	66
32	UART Topology.....	70
33	SPI0 Topology.....	74
34	SPI1 Topology.....	75
35	Clock Integration Distribution Diagram .....	79
36	Differential Clock Topology for SoC to Clock Receiver .....	81
37	Single Ended Clock Topology for SoC .....	82
38	25 MHz Crystal External Load Capacitor Parameters .....	85
39	Legacy SPI Topology (Single Device).....	88
40	SPI Single Flash Device Routing Guidelines for LSPI0_MOSI, LSPI0_MISO, LSPI0_CS_N,LSPI0_SCK.....	88
41	SPI Topology (4 SPI Devices + Legacy SPI Device) .....	90
42	RTCX1 and RTCX2 Relationship in SoC .....	93
43	Example External Circuitry for the SoC RTC.....	95
44	A Schottky Diode Circuit to Connect RTC External Battery .....	98
45	RTCRST# External Circuit for the SoC RTC .....	99
46	Example GPIO[7:0] Topology level shifted Guideline .....	102
47	Generic GPIO[7:0] Topology Guideline .....	102
48	Intel® Galileo Platform Power Delivery .....	106
49	Intel® Quark SoC X1000 Power-up Sequence .....	107
50	platform_s5_pwrok generation .....	111
51	Power Sequence Timing .....	112



52	Time Domain Capture of Exerciser Operation .....	116
53	Current Loop Radiation of a Transmission Line .....	117
54	Radiation Cancellation of a Differential Line .....	118
55	An Example of VR EMI Noise.....	119
56	VR Noise Can Result In Both SI and EMI Issues.....	119
57	Simplified Voltage Regulator Module Circuit and VRM EMI Noise .....	119
58	The Vx Ripples with/without Gate Resistors (Left: without gate resistor/ Right: with gate resistor) .....	120
59	Emission from a Differential line with Various Skews .....	121
60	Changing Referencing, Lack of Referencing, Void-crossing, and Split-crossing are Not Recommended.....	122
61	Signal Traces Should be away from Plane Edges.....	122
62	Keep-out Zone Determined Around IO and Other Connectors .....	123
63	Simple Capacitor Model and an Example of Capacitor Impedance .....	123
64	Stitching Capacitors Could Create Low Impedance Path for Return Currents .....	124
65	Stitching Capacitors Mitigate EMI (Simulated Results) .....	125
66	Stitching Capacitors Should be Close to Traces.....	126
67	Decoupling Capacitors Locations .....	126
68	Decoupling Capacitors with Vias .....	127
69	Decoupling Capacitors Around the Edges of Power Plane .....	127
70	USB 2.0 Common Mode Choke.....	128
71	Demonstration of Spread Spectrum Clocking (SSC) .....	129
72	Spectral Comparison of a Clock Scrambled vs. Unscrambled .....	130
73	Ground Vias Placement .....	131
74	Cable/Adaptor Shielding Impacts EMI Significantly.....	132
75	IEC 61000-4-2 ESD Waveform.....	136
76	Mutual L and C (Lm, Cm) Coupling .....	137
77	Ground Shape Along the I/O Edge of the Board.....	138
78	Series RC Filter for ESD Mitigation on Asynchronous Nets .....	139
79	Frequency Response of The Series RC Filter.....	139
80	ESD Noise Suppression Using Series RC Filters.....	140
81	Signal Integrity Analysis With Series RC Filters .....	141
82	Circuit Diagram of Direct Injection Method .....	142
83	USB 2.0 ESD Protection Devices.....	143
84	Typical Integrated Diode Array Package .....	143
85	Layout Example of USB 2.0 with ESD Diode Array .....	144
86	Differential S-parameters from Ceramic 1-line, Si 4-line and Si 6-line ESD Protection Devices.....	145
87	Example of Test Bead on a Stub (Not Preferred).....	150
88	Example of Differential Test Bead with Matched Placement .....	150
89	Bead Formed Over Solder-Mask Opening.....	151
90	Bead Placed on Existing Via .....	152
91	SOC/PHY Interface Connections .....	153
92	LED Hardware Configuration .....	158
93	Single PHY Solution Interconnect .....	159
94	PLC Placement: At Least One Inch from I/O Backplane.....	161
95	Effect of LAN Device Placed Too Close To a RJ-45 Connector or Chassis Opening .....	161
96	MDI Trace Geometry .....	164
97	MDI Differential Trace Geometry .....	165
98	Trace Transitioning Layers and Crossing Plane Splits.....	167
99	Via Connecting GND to GND .....	168
100	Stitching Capacitor between Vias Connecting GND to GND .....	168
101	Ideal Ground Split Implementation .....	169
102	Ground Layout with USB .....	170
103	Typical ePAD* Land Pattern .....	192



104 Typical Thermal Pad and Via Recommendations .....	192
105 Recommended Thermal Via Patterns .....	193
106 Stencil Design Recommendation .....	194
107 Assembly Flow .....	194
108 Typical Profile Band .....	195



## Tables

1	Platform Stack-up Parameter Values (Microstrip).....	20
2	Electrical Limits of LH Material Properties .....	22
3	Breakout Geometries for Various I/O Interfaces .....	25
4	Max Root Square Sum (RSS) Length vs. Transfer Speed.....	27
5	This Guideline Supports the Following Configurations .....	31
6	DDR3 Channel Signal Groups.....	32
7	Memory Channel Signals Groups Routing.....	32
8	DQ/DQS Routing Guidelines and Settings for a Single Rank 4L Fly-by Design - PCB Type 3	33
9	Control - Routing Guidelines and Settings for a Single Rank 4L Fly-by Design - PCB Type 3	35
10	Command Routing Guidelines and Settings for a Single Rank 4L Fly-by Design - PCB Type 3	36
11	Clock Routing Guidelines and settings for a Single Rank 4L Fly-by Design - PCB Type 3	38
12	Precision Resistor Value for DDR_XXXPU Compensation Inputs .....	41
13	PCI Express* Root Ports Speed Support .....	43
14	PCIe* Root Ports 1 and2 Supported Configurations .....	43
15	SoC PCI Express* Compensation and Voltage Reference Guidelines .....	45
16	PCI Express* Reference Documents.....	45
17	PCI Express* Signal Groups (Standard Card) .....	45
18	PCI Express* Card Topologies.....	46
19	PCI Express* Expansion Card Routing Tx to Connector.....	47
20	PCI Express* Expansion Card Routing Rx to Connector.....	48
21	Signal Groups.....	52
22	USB 2.0 External Routing Guidelines MicroUSB.....	54
23	USB 2.0 External Routing Guidelines Mini PCIe* .....	55
24	I <sup>2</sup> C Signals.....	61
25	I2C* Signal Routing Summary .....	62
26	Bus Capacitance Reference Chart .....	64
27	Example Bus Capacitance/Pull-Up Resistor Relationship.....	64
28	SDIO Signals.....	65
29	SDIO Layout Guideline.....	66
30	SOC SDIO Pull Up/Down .....	67
31	UART Signals.....	69
32	UART Routing Guideline .....	70
33	UART Internal Pull Up/Down .....	70
34	SPI Signals .....	73
35	SPIO_MOSI, SPIO_SCK .....	74
36	SPIO_MISO .....	74
37	SPI1_MOSI, SPI1_SCK .....	75
38	SPI1_MISO .....	76
39	SOC SPI Internal Pull Up/ Pull Down .....	77
40	Signal Groups.....	80
41	Differential Clock Routing Guidelines.....	81
42	iClock (Single-ended Clocks) .....	83
43	SPI Signals .....	87
44	LSPIO_MOSI, LSPIO_MISO, LSPIO_CS_N, LSPIO_SCK .....	88
45	RTC Signals.....	93
46	RTC Routing Guidelines.....	95
47	RTC External RTCRST# Routing Guidelines .....	99
48	Asynchronous Legacy Signal Group .....	101
49	Asynchronous Signal General Routing Guideline .....	102
50	GPIO[7:0] General Routing Guideline.....	102
51	Recommended Platform Power Delivery .....	105
52	Platform Reset Signals.....	109



53	Critical Signals .....	113
54	Critical Signals Routing Summary .....	114
55	Frequency Sensitivity .....	114
56	Component Placement Review Checklist .....	133
57	General Routing Review Checklist .....	133
58	I/O Routing Review Checklist .....	134
59	Decoupling/Filtering Review Checklist.....	134
60	Tested Sensitive Nets.....	142
61	ESD Checklist .....	146
62	JTAG PullUp / PullDown Requirements .....	148
63	Bead Parameters.....	150
64	MDIO Data Signals on the Intel® Quark SoC X1000 .....	154
65	RMII Signals .....	154
66	Clock and Reset Signals .....	154
67	Integrated Magnetics Recommended Qualification Criteria.....	156
68	MDI Routing Summary .....	162
69	Maximum Trace Lengths Based on Trace Geometry and Board Stack-Up .....	163
70	Capacitor Stuffing Option Recommended Values .....	170
71	MAC0_TXDATA<1:0>; MAC0_TXEN; MAC0_MDC; MAC0_MDIO.....	173
72	MAC0_RXDATA<1:0>; MAC0_RXDV.....	173

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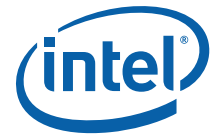


## Revision History

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Revision	Description	Date
001	Initial Public Release	March 2014

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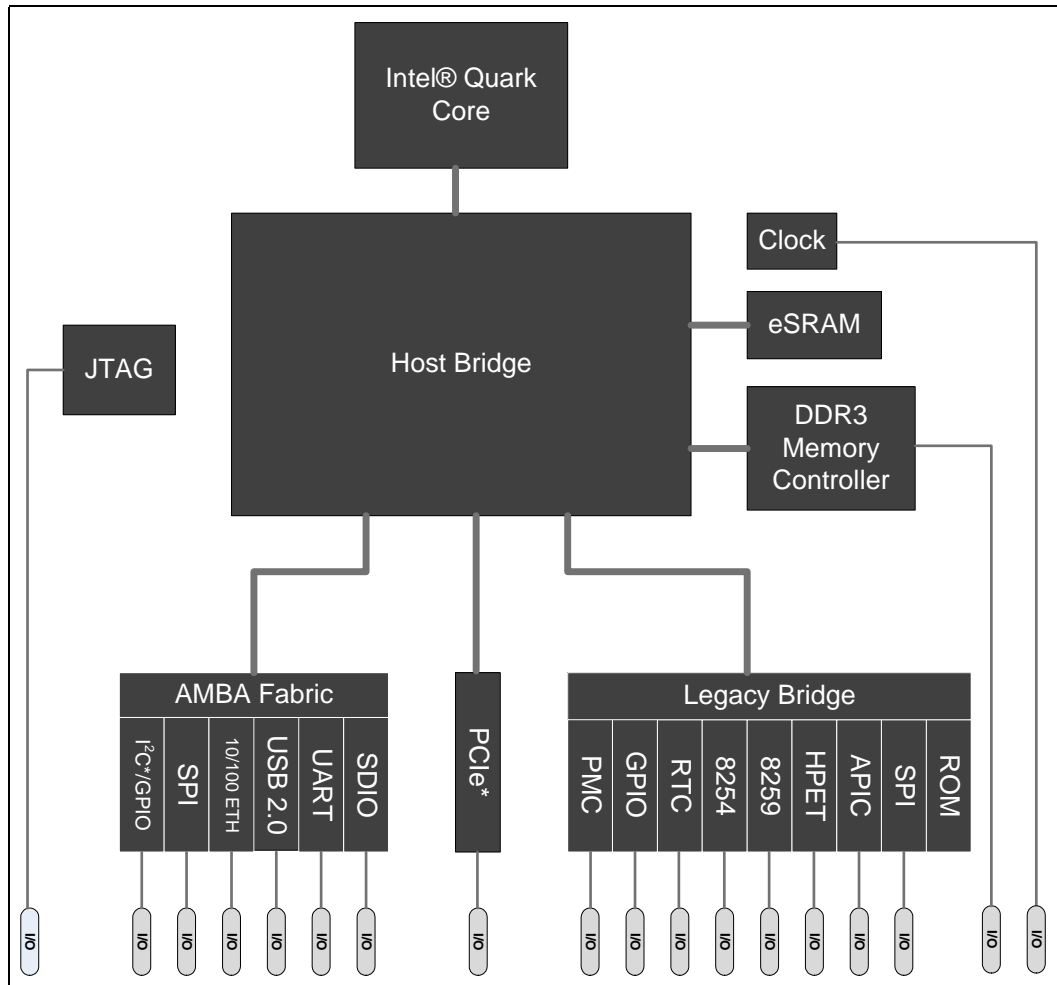
## 1.0 Introduction

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This Design Guide provides motherboard implementation recommendations for a platform based on the Intel® Quark SoC X1000 processor. *The Intel® Quark SoC X1000 Platform Design Guide* has been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. Design recommendations are based on Intel's simulations and lab experience and are strongly recommended, if not necessary, to meet the timing and signal quality specifications. Design recommendations are based on the reference platforms designed by Intel. They should be used as an example but may not be applicable to particular designs.

The guidelines recommended in this document are based on experience, simulation, and preliminary validation work done at Intel while developing the Intel® Quark SoC X1000-based platform. This work is ongoing, and these recommendations are subject to change. Metric units are used in some sections in addition to the standard use of U.S. customary system of units (USCS). If there is a discrepancy between the metric and USCS units, assume the USCS unit is most accurate. The conversion factor used is 1 inch (1000 mils) = 25.4 mm.

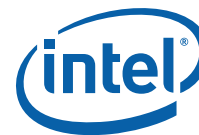
Figure 1. Intel® Quark SoC X1000 Block Diagram



## 1.1 Terminology

Term	Description
DPFT	Dynamic Platform & Thermal Framework; includes configurable TDP and Low Power Mode.

§ §



## 2.0 Stack-Up and PCB Considerations

---

*Note:* Metric units are used in some sections in addition to the standard use of U.S. customary system of units (USCS). If there is a discrepancy between the metric and USCS units, assume the USCS unit is most accurate. The conversion factor used is 1 inch (1000 mils) = 25.4 mm.

### 2.1 Printed Circuit Board (PCB) Considerations

Several layer count configurations may be implemented on the platform, provided the trace geometries of the individual microstrip and stripline routing layers fall within the parameter value ranges and the impedance specifications are met. It is important to note that variations in the stack-up of a motherboard, such as changes in the dielectric height, trace widths, and spacing, can impact the impedance, loss, and jitter characteristics of all the interfaces. Such changes may either be intentional or the result of variations encountered during the PCB manufacturing process. In either case, they must be properly considered when designing interconnects.

The following figures depict the set of geometry metrics associated with the external (microstrip) routing and dual-stripline routing layers for both single-ended and differential signals. The typical values and simulation sweep ranges for each parameter are defined in the following tables. If motherboard parameters (including manufacturing variances) fall outside of the boundaries shown, perform additional simulations to ensure proper signal integrity and specification compliance.

- Design tolerances account for adjustments intentionally included in their design.
- Material tolerances account for any natural variation in the materials being used.
- Manufacturing tolerance considers variations that may occur during the manufacturing process.
- Use the design tolerance to recenter stack-up impedance, but consider the manufacturing tolerance impact when comparing the chosen stack-up to the given recommendation.

The typical values, including the design and material tolerances, are centered around a nominal single line impedance specification of  $50 \Omega \pm 15\%$  for microstrip. Many interfaces specify a different nominal single-ended impedance. For more details on the nominal trace width to hit those impedance targets, refer to the individual interface section.

The following general stack-up recommendations should be followed:

- Microstrip layers are assumed to be built from  $\frac{1}{2}$  oz. foil, plated up nominally another 1 oz., however, the trace thickness range defined allows for significant process variance around this nominal.
- All high-speed signals should reference solid planes over the length of their routing and should not cross plane splits. Ground referencing is preferred.
- Reference plane stitching vias must be used in conjunction with high-speed signal layer transitions that include a reference plane change. Refer to each signal group section for more specification.

- The parameter values for internal and external traces are the final thickness and width after the motherboard materials are laminated, conductors plated, and etched. Intel uses these exact values to generate the associated electrical models for simulation.
- Avoid any signal routes or components (e.g., resistors) in the processor cavity to avoid potential EMI interference with the processor package. This routing restriction applies to the top layer only; it is okay to route signals in the processor cavity on the inner and bottom layers.

Figure 2. Single-Ended Microstrip Diagram

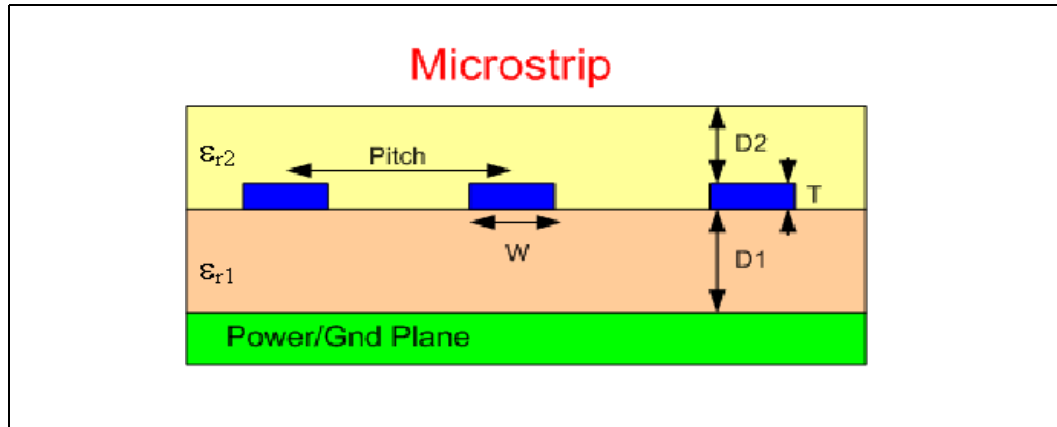


Figure 3. Differential-Microstrip Diagram

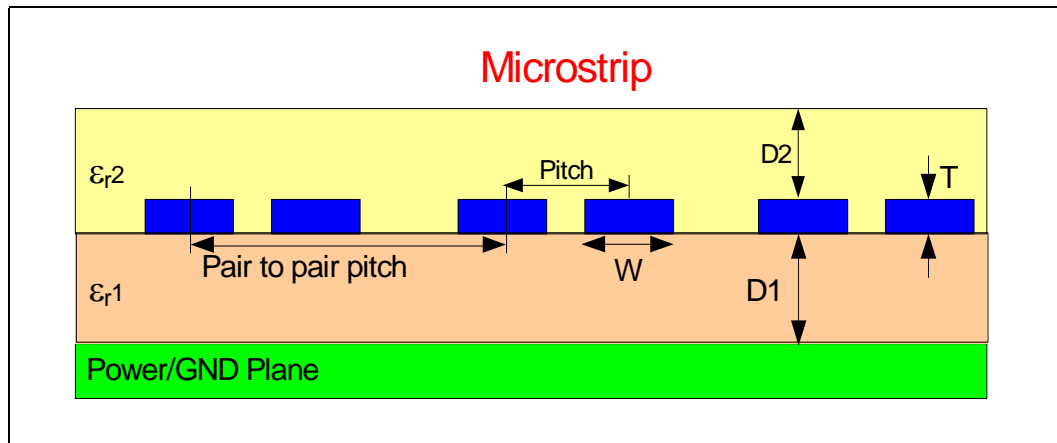
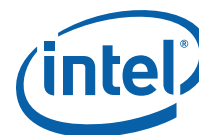


Table 1. Platform Stack-up Parameter Values (Microstrip) (Sheet 1 of 2)

Microstrip	Units	Min Value	- Manufacturing Tolerance	- Design/ Material Tolerance	Typical Value	+ Design/ Material Tolerance	+ Manufacturing Tolerance	Max Value
D1	mils	2.05	0.3	0.4	2.75	0.2	0.3	3.25
D2	mils	0.1	0.3	0.25	0.65	0.25	0.30	1.20
$\epsilon_{r1}$	NA	3.45	0.15	0.3	3.9	0.3	0.15	4.35
$\epsilon_{r2}$	NA	3.20	0.2	0	3.40	0	0.2	3.60
Trace Thickness (0.5 oz. Plated)	mils	1.30	0.28	0.32	1.90	0.32	0.28	2.50


**Table 1. Platform Stack-up Parameter Values (Microstrip) (Sheet 2 of 2)**

Microstrip	Units	Min Value	- Manufacturing Tolerance	- Design/ Material Tolerance	Typical Value	+ Design/ Material Tolerance	+ Manufacturing Tolerance	Max Value
Trace Width (Bottom)	mils	3.1	0.40	0.5	4.00	0.25	0.40	4.65
Trace Width (Top)	mils	2.1	0.40	0.5	3.00	0.25	0.40	3.65

## 2.2 Low Halogen Flame Retardant Stack-Up Considerations

### 2.2.1 Low Halogen Background

FR4 epoxy has been used in the construction of PCBs for decades. Consequently, its electrical properties, which are influenced by brominated flame retardants integrated into the molecular structure of the resin, have been studied extensively. As an environmentally friendly alternative to the halogenated flame retardants in FR4, several new low halogen (LH) formulations were developed by different material suppliers. Unfortunately, each new formulation has a unique electrical performance that differs from FR4. This leads to the current problem: The critical electrical properties of many LH dielectrics currently on the market make it difficult to design high-speed buses without increasing the cost of the system. The range of supported  $\epsilon_r$  values therefore limits the amount of cost added.

The most apparent problem lies with the increased permittivity of the LH dielectric materials compared to FR4. Measurements show that several LH PCB materials on the market can have permittivity values around 5 at 1 GHz (using 1080 glass), while FR4 has permittivity values in the 3.6 - 3.9 range. Increased permittivity requires thicker dielectric layers to achieve the equivalent impedance as FR4. In turn, the thicker dielectric layers lead to an increase in crosstalk which reduces bus performance. If the trace-trace spacing and line widths remain constant (consequently board area consumed remains constant), and the dielectric thickness is adjusted to maintain constant characteristic impedance, the bus performance is reduced for high permittivity values due to increased crosstalk.

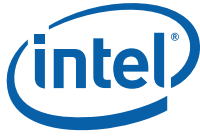
Conventional means of reducing crosstalk is to isolate traces as much as practical to reduce the electromagnetic coupling of energy. Unfortunately, modern motherboard designs are often real-estate constrained, requiring extra layers (and therefore cost) to provide additional space for crosstalk compensation when using high permittivity dielectrics.

### 2.2.2 Choosing a Low Halogen Material

Choosing an LH dielectric material for a specific design requires a compromise between performance and cost, especially when a single design is required to work with both LH and FR4 PCB materials. Consequently, it is impossible to define universal requirements for LH dielectrics that will be adequate for all products on the market. Generally speaking however, the dielectric materials used to design printed circuit boards (PCBs) with high-speed digital interfaces perform better with low permittivity and low losses. Low permittivity tends to reduce crosstalk noise for given impedance and low loss tangents reduce signal attenuation.

### 2.2.3 Electrical Limits of Low Halogen Material Properties

Although it is impossible to define electrical limits to universally select “good” materials versus “bad” materials because each design is unique in its implementation, general limits can be chosen that will be adequate for most applications. Simulations were



performed on several high-speed buses and validation platforms were built to help identify electrical limits of LH materials that will help ensure 1) adequate bus performance and 2) interchangeability between FR4 and LH material. The layout constraints listed in this document have been designed to function with both standard FR4 and LH materials if the electrical properties of the LH materials fall within the envelope defined by Table 2.

Table 2. Electrical Limits of LH Material Properties

Parameter	Approximate LH Electrical Limits	Environmental Condition
Permittivity (Er)	<4.2 (1080, RC~61%) <4.3 (RC~50%) <4.5 (2116, RC~45%)	Any environmental conditions
Loss Tangent (tanδ)	<0.018 (1080, RC~61%) <0.014 (1080, RC~50%) <0.013 (2116, RC~45%)	50% RH & 75oF
Moisture Impact on Loss (tanδ)	<0.024(1080, RC~61%) <0.019(RC=50%) <0.017 (2116, RC~45%)	95% RH & 95oF

**Note:** Approximate limits of desired electrical performance of LH dielectric materials; RC =% Resin Content, RH = Relative Humidity; 1080 stackups have between ~ 60-65% resin content depending on the layer thickness; Limits established using buses implemented on 1080 material. 2116 (RC=45%) and RC=50% limits extrapolated from the 1080 data points using the volume ratio of resin to glass and average values of resin density, glass density, glass permittivity, glass tan and glass weight basis.

Although the limits listed in Table 2 are generally lower performance than standard FR4, simulated and measured data indicate that they are sufficient to ensure proper functionality of the buses listed in this design guide. Since the volume of LH materials on the market is small compared to FR4, the performance envelope was made as large as practical to maximize the number of LH materials that comply without significantly sacrificing signal integrity. Table 2 does not guarantee equal performance to FR4. However, if the limits are adhered to, then the risk of signal integrity problems due to the LH material is greatly reduced. Intel bases signal integrity analysis and validation on these ranges.

Designers should also ensure the LH dielectric materials chosen meet all applicable thermal, mechanical and UL flammability requirements.

### 2.3 Reference Planes

- Reference all signal routing layers to a solid ground plane that is continuous over the length of the interconnect. Specific requirements may be defined within the interface design guideline chapters.
- Using a power layer as a reference plane is allowed if the power layer is low noise and there is proper decoupling stitching at reference planes transitions to guarantee high frequency return path continuity. However, this should only be considered as the secondary reference plane on internal layers where a solid continuous ground reference is already present. Even in this case the power plane must be low noise due to the possibility of noise being coupled into the associated signal planes.
- Route noisy power planes, such as VBAT, on the same layers as signals to minimize fringe coupling by proper spacing separation.

### 2.4 Backward and Forward Coupling Coefficient Calculation

Some designs require a stack-up build that is outside of the ranges provided. In this case, compare the routing electrical characteristics versus the Intel recommendation.



Comparing the single-ended and differential-impedances is important. However, crosstalk level, which is governed by trace spacing, is not implied by the impedance target. Calculating and comparing backward coupling coefficients is recommended to choose proper trace spacing in cases where the selected stack-up varies from the Intel recommendation.

The coupling coefficients represent the source voltage percentage that is coupled to victim lines. As shown in Figure 4,  $K_b$  is defined as the backward coupling coefficient. For backward (near-end) crosstalk, inductive and capacitive coupling are of the same polarity and the noise magnitude is not a function of trace length. The backward coupling coefficient ( $K_b$ ) values can be used to decide trace spacing.

For forward (far-end) crosstalk,  $K_f$  inductive and capacitive coupling are of opposite polarity and the crosstalk magnitude ( $V_{fe}$ ) is proportional to both trace length and edge rate.  $K_f$  is typically a very small value in most practical designs. Therefore, Intel has not included the  $K_f$  values in the Design Guide. However, the equation for calculating  $K_f$  is provided in Figure 5 if the value is desired.

$K_b$  values for all interfaces for all routing layers can be found in Table 3 and Table 4. They were calculated assuming a nominal or typical stack-up configuration based on the values in Table 1 to Table 4. For single-ended interfaces, the  $K_b$  values reflect the crosstalk seen between each typical spacing. For typical spacing differential interfaces, the  $K_b$  values reflect the crosstalk seen between each differential pair based on the typical pair-to-pair spacing.

Figure 4. Backward Coupling Coefficient

$$K_b = \frac{1}{4} \left( \frac{|C_{ij}|}{\sqrt{C_{ii}C_{jj}}} + \frac{|L_{ij}|}{\sqrt{L_{ii}L_{jj}}} \right)$$

$$V_{NE} = K_b \bullet V_0$$

Figure 5. Forward Coupling Coefficient

$$K_f = \frac{1}{2} \left( \frac{|C_{ij}|}{\sqrt{C_{ii}C_{jj}}} - \frac{|L_{ij}|}{\sqrt{L_{ii}L_{jj}}} \right) (L_{ii}C_{ii}L_{jj}C_{jj})^{1/4}$$

$$V_{FE} = K_f \bullet Length * \frac{dV}{dt}$$

Figure 6. Single-ended Kb Diagram

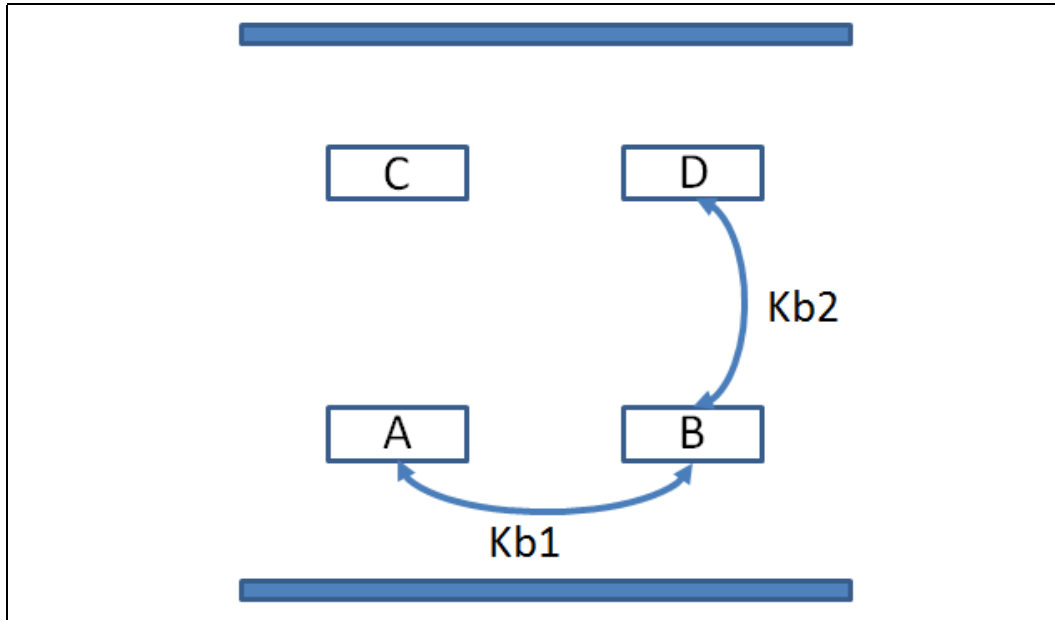
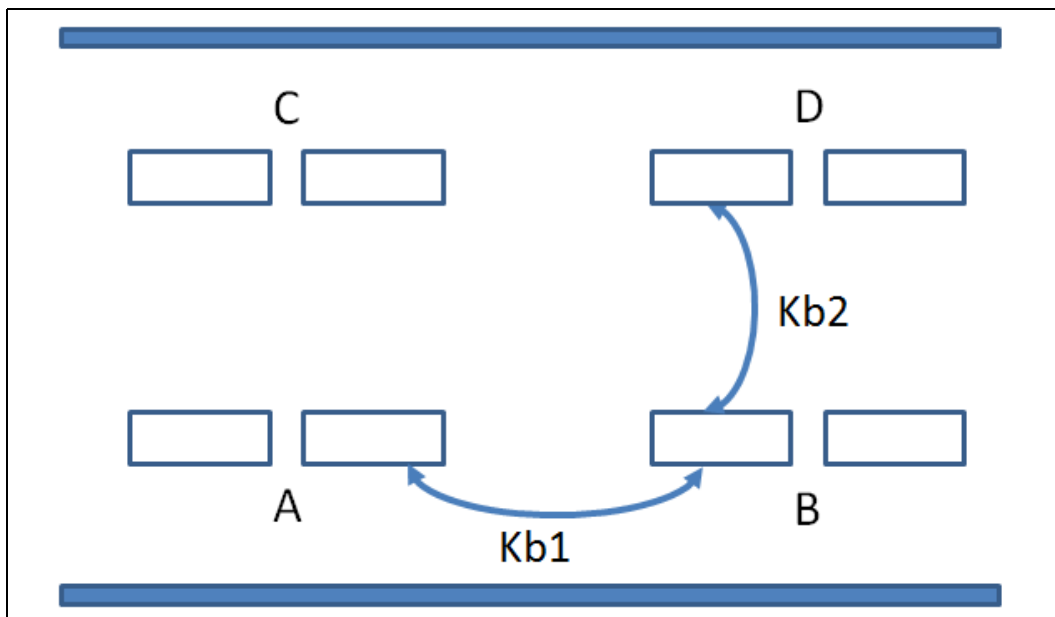


Figure 7. Differential Kb Diagram



## 2.5 Single-Ended and Differential-Impedance Transmission Line Specifications

Table 3 lists breakout trace geometries for various I/O interfaces. Breakout topologies are mainly decided by package ballout patterns and pitches. So similar geometries will be used for various stack-ups. Refer to interface chapters for the breakout maximum length allowed and signals not listed in this table.

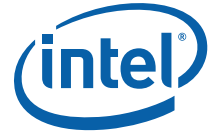


Table 4 lists examples of single-ended and differential impedances specified for different interfaces. The microstrip single-ended impedance tolerance is  $\pm 15\%$ . The stripline and dual-stripline single-ended impedance and differential impedance tolerance is  $\pm 10\%$ . The microstrip differential-impedance tolerance is  $\pm 15\%$ .

**Table 3. Breakout Geometries for Various I/O Interfaces**

I/O Interfaces	Component	Stack-Up	Units	Trace Width	Minimum Trace Spacing	Minimum Pair-to-Equivalent Pair Spacing <sup>1</sup>	Minimum Pair-to-Non-Equivalent Pair Spacing <sup>1</sup>
USB2/ PCIe/ Platform Clocks	SOC	MS	mils	4	4	8	8
DDR3	SOC	MS	mils	4	4	NA	NA
Default <sup>2</sup>	SOC	MS	mils	4	4	NA	NA
	SOC	MS	mils	3.5	4	NA	NA

**Notes:**

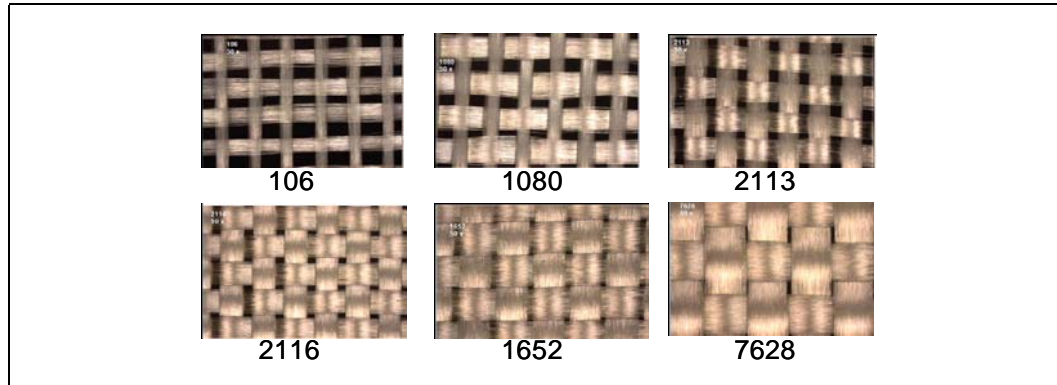
1. Equivalent pairs mean both pairs have equal swing and signal propagation direction. Non-equivalent pairs mean both pairs have different swing or propagation direction.
2. Default refers to legacy signals which are not listed in the table, i.e., low speed non-critical signals.

## 2.6 Minimizing the Effect of Fiber Weave

### 2.6.1 Overview of Fiber Weave

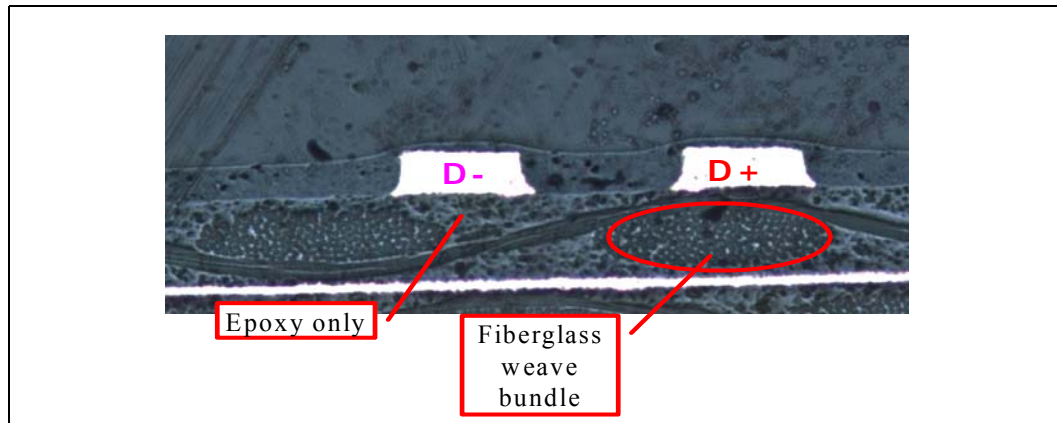
Fiber weave in the PCB material impacts the routing of high-speed traces. The PCB material is made up of a composite of fiber and resin. The strands of fiber run perpendicular to each other. Depending on the orientation of the weave relative to the trace, there could be either resin or a fiber bundle beneath the trace. Due to the differing dielectric constants of these two materials, a phase skew could be introduced among signals that comprise a differential pair. This phase skew manifests itself as an AC common mode noise at the receiver, affecting both voltage and timing margin at the receiver. The layout recommendations in this section will minimize the effect of the PCB fiber weave on the routing of differential signals. The choice of a particular mitigation technique is dependent on the configuration and layout of the platform and, hence, this choice is left to the platform designer. Typical printed circuit boards, due to their basic construction consisting of woven fiberglass fabric ( $E_r \sim 6$ ) strengthened and bound together with epoxy resin ( $E_r \sim 3.5$ ), present a non-homogeneous medium for signal propagation of differential pairs. As shown in Figure 8, there are several weave types, with the weave strands running horizontal and vertical relative to the board edges. For differential pairs with trace width and spacing comparable to the dimensions of the fiberglass cloth, the PCB's non-uniform dielectric can give rise to substantial propagation differences between the conductors of the pair, see Figure 9.

Figure 8. Common Glass Cloths Used in PCB Manufacture



**Note:** Weave types above are for illustration purposes only

Figure 9. Inhomogeneous Nature of a PCB as Shown in this Cross-Section



**Note:** Note the fiber weave bundle and epoxy regions

At high data rates this skew can amount to a substantial fraction of the transmission unit interval, resulting in an increased common mode voltage and a correspondingly degraded differential signal (Figure 10). In addition, the resulting common mode signal (ACCM) can become a source of increased crosstalk and EMI in the system, or violate receiver ACCM specifications.



Figure 10. Effect of Skew on Differential and Common Mode Signals

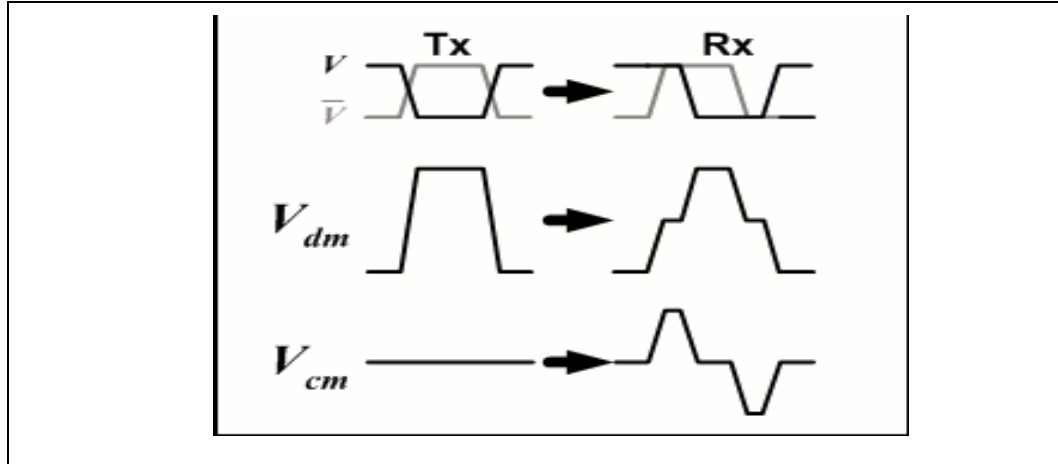
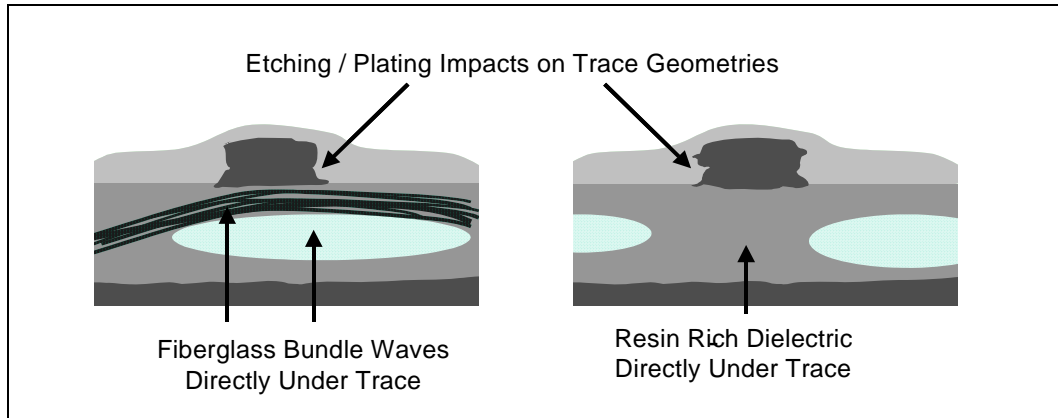


Figure 11. Cross-Section of PCB Indicating Effect of PCB Fiber Weave



Fiber weave effect is noticeable for routing lengths greater than 2" and this effect gets more pronounced for longer trace lengths. There are many approaches to minimize this effect and the next three sections suggest some methods to mitigate this effect. The AC common mode noise causes considerable degradation of the signal for trace lengths in the range of 5" to 15" for a typical PCB stackup on FR4 material.

### 2.6.2 Fiber Weave Effect versus Transfer Rate and Trace Length

Table 4. Max Root Square Sum (RSS) Length vs. Transfer Speed

Transfer Speed	Max RSS length (See note 1)
2.5 GT/s	5"
4 GT/s	4"
5 GT/s	3"
6.4 GT/s	2.5"
8 GT/s	2"

**Notes:**

- The lengths in the table represent total trace lengths that are aligned to the weave (i.e., parallel to the manufacturing panel's edge). Actual routing may have a significant portion of the length at angles to

the edge of the board. Those lengths should not be considered in this analysis.

The total length is the Root Square Sum of total vertical and horizontal lengths that run parallel to the weave:

$$\text{Length} = (H_1)^2 + (H_2)^2 + (H_3)^2 + (V_1)^2 + (V_2)^2 + (V_3)^2 + \dots$$

where:  $H_x$  = length of each segment routed horizontally, and  
 $V_x$  = length of each segment routed vertically

2. The table represents an approximation only, based on simulations of “representative” topology. The exact fiber weave may vary, depending on the exact topology.

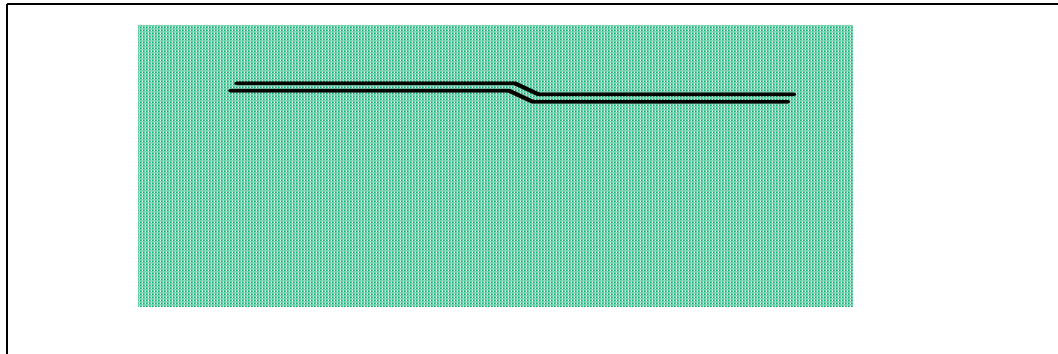
### 2.6.3 Specific Routing Configurations

Some platforms might have their components laid out in a manner that requires non-orthogonal (to the PCB board edge) routing for their high-speed busses. Orthogonal routing up to a maximum length of 2” does not result in a noticeable impact on the differential signals. However, there could be a significant amount of AC Common-Mode voltage introduced between the differential pair that the platform designer will need to consider.

### 2.6.4 Offset Routing

This involves routing the trace in a straight line with offset in the middle equal to a glass bundle pitch. The glass bundle pitch differs by materials and direction and is dependent on the particular manufacturing process. An example is shown in [Figure 12](#). For this technique to be applied, a PCB layout tool with this capability would be required.

Figure 12. An Example of Offset Routing



### 2.6.5 Zig-Zag or Slanted Routing

If the weave is aligned to the PCB edges, follow a zig-zag or slanted routing of differential traces. Maintain a minimum angle of 10 degrees between the trace and fiber weave. This will lead to traces that are angled relative to the PCB edge. [Figure 13](#) is an example of zig-zag routing. [Figure 14](#) shows slanted routing. For this technique to be applied, a PCB layout tool with this capability would be required.

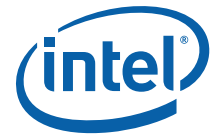


Figure 13. An Example of Zig-Zag Routing

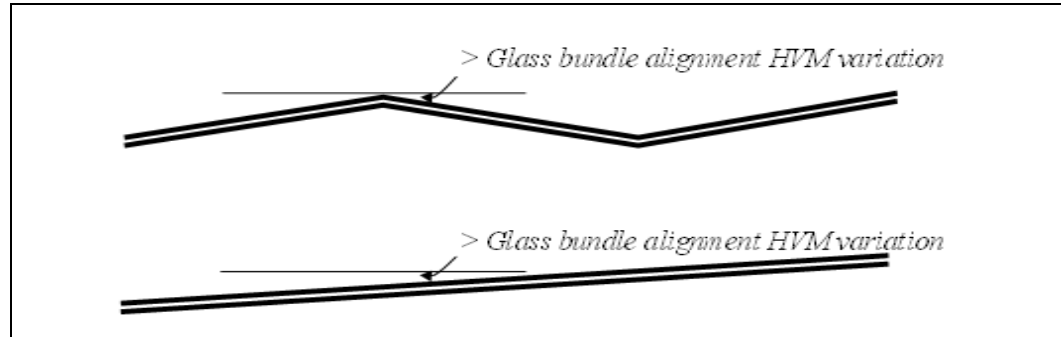
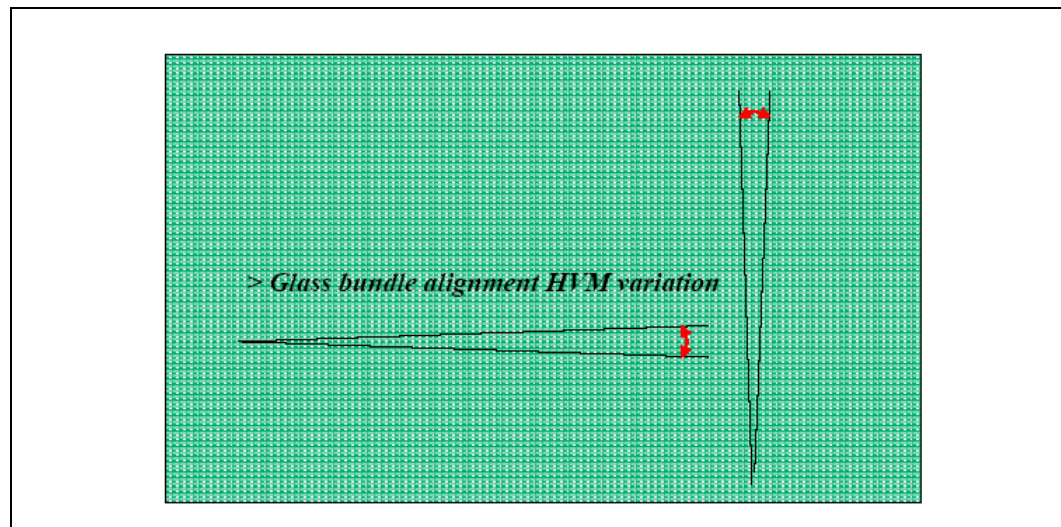


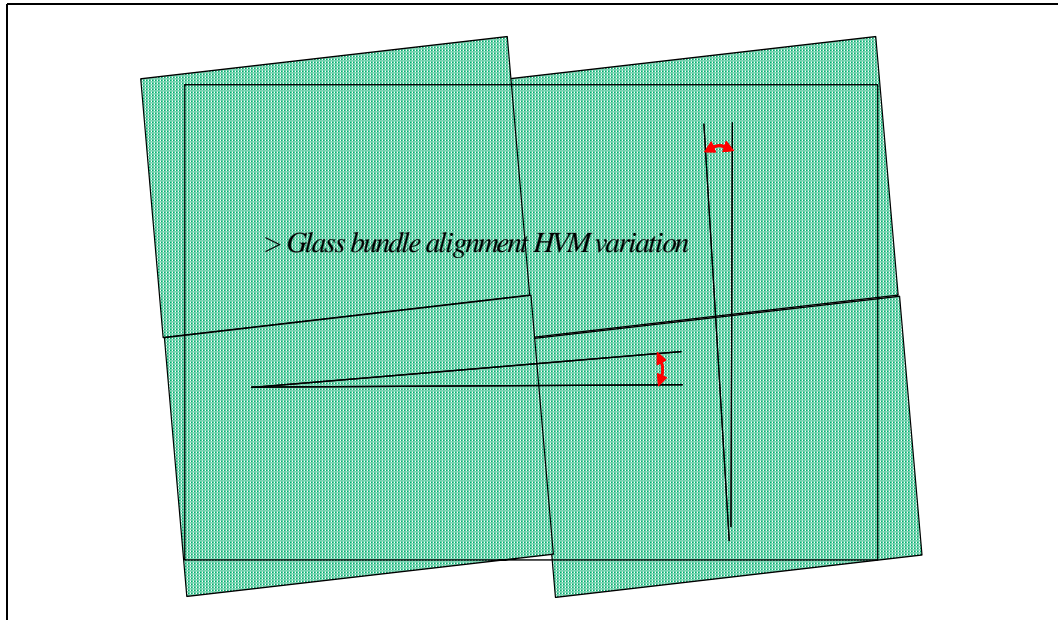
Figure 14. An Example of Slanted Routing



### 2.6.6 Image Rotation

Another solution is to maintain an angle between the trace and the fiber weave pattern is to rotate the weave relative to the edge of the PCB, thereby maintaining differential trace routes aligned with edges of the PCB (refer [Figure 15](#)). It is recommended the rotation be such that the traces are at a 10 degree angle relative to the fiber weave. The rotation can be achieved by cutting the PCB board at an angle, as shown in [Figure 15](#), or by rotating the layout database relative to the edge of the PCB board. The latter requires the use of an appropriate PCB routing software that has this capability.

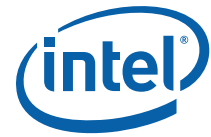
Figure 15. An Example of a PCB Cut Such That Its Edges are Rotated Relative to the Fiber Weave Pattern



### 2.6.7 Using Alternate PCB Materials

The fiber weave effect can also be minimized by using PCB material that exhibits less variation in the dielectric coefficient  $E_r$  between the epoxy and glass materials.

§ §



## 3.0 DDR3 Memory Design Guidelines

### 3.1 Memory General Introduction

Intel® Quark SoC X1000 Customer Reference Board (codename Kips Bay) platforms support DDR3 memory technology. The CRB's SoC memory interface supports a single-channel of DDR3 memory with 8-bit wide data and up to 2 ranks per channel at 800 MT/s.

This document covers the guidelines to design a Kips Bay platform memory subsystem using Memory Down approach.

#### 3.1.1 Supported Memory Configurations

Table 5. This Guideline Supports the Following Configurations

Parameter	1 Rank/Channel	2 Ranks/Channel
Supports up to:	DDR3-800	DDR3-800
Device Densities Supported	1Gb, 2Gb, 4Gb	1Gb, 2Gb, 4Gb
Device Widths Supported	x8	x8
Memory capacity	256MB-1GB	512MB-2GB
PCB Layers	4L	TBD

#### 3.1.2 Memory Population Rules

Rank0 is mandatory; Rank1 is optional; All devices must be of the same bit density.

#### 3.1.3 Reference Documents

See JEDEC Standard for DDR3 SDRAM Specification at <http://jedec.org>.

DDR3 TLC (Trace Length Calculator):  
*Clanton\_DDR3\_4L\_single\_rank\_fly\_by\_topology\_Trace\_Length\_Calculator\_rev\_0\_4\_Draft.xlsm* - external version CDI# 523409

#### 3.1.4 Design Constraints-based Routing

Design constraints need to be derived from all of the following sections:

- Memory Stackup Guidelines
- Stackup and Layer Utilization Guidelines
- Memory Block Diagram and Connectivity
- Memory Bit swapping and Byte Lane swapping
- Memory Length Matching Guidelines



- Compensation
- Voltage Reference Rules

### 3.2 Memory Signal Description

Table 6. DDR3 Channel Signal Groups

Signal Name	Description
Clock Signal Group	
DDR3_CK[0], DDR3_CKB[0]	Differential Clock pair for Rank0
DDR3_CK[1], DDR3_CKB[1]	Differential Clock pair for Rank1
Control Signal Group (signals per rank)	
DDR3_CSB[1:0]	Chip Select (One per rank)
DDR3_CKE[1:0]	Clock Enable (One per rank)
DDR3_ODT[1:0]	On-Die Termination Enable (One per rank)
Command Signal Group (common across ranks)	
DDR3_MA[15:0]	Memory Address Bus
DDR3_BS[2:0]	Bank Select
DDR3_RASB	Row Address Select
DDR3_CASB	Column Address Select
DDR3_WEB	Write Enable
Data Signal Group (common across ranks)	
DDR3_DQ[15:0]	Data Bus
DDR3_DQS[0], DDR3_DQSB[0]	Data Strobe for DQ[7:0]
DDR3_DQS[1], DDR3_DQSB[1]	Data Strobe for DQ[15:8]
Miscellaneous	
DDR3_DRAMRSTB	Reset for all DRAM devices

Table 7. Memory Channel Signals Groups Routing

Parameter	Clock	Control	Command	Data	Data Strobe
Motherboard Topology	Differential-Pair Point-to-Point	Point-to-Point	Point-to-Point	Point-to-Point	Differential-Pair Point-to-Point
Reference Plane	Dual Referenced GND & PWR	Dual Referenced GND & PWR	Dual Referenced GND & PWR	Dual Referenced GND & PWR	Dual Referenced GND & PWR

*Note:* It is recommended that all of the signals have solid GND referencing planes on both sides. Minimize the size of void if there are voids on reference planes.

### 3.3 Memory Topology Guidelines

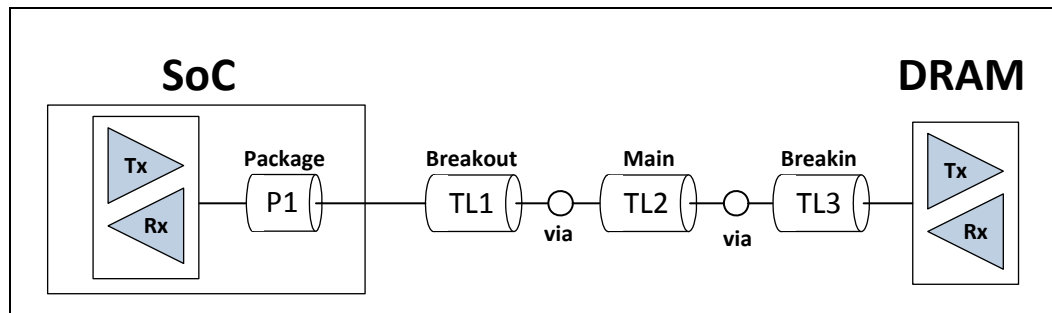
This chapter presents the various DDR3 topologies possible with Intel® Quark SoC X1000 platforms and associated constraints for PCB layout.



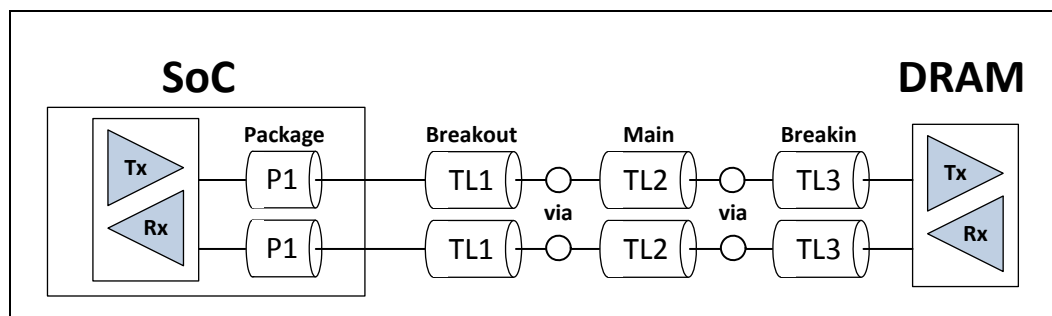
### 3.3.1 Single Rank Fly-by Topology with Active VTT Termination

The topology presented in this chapter is the basic DDR topology for 4 Layer PCB designs. For PCB stack-up information please refer to [Chapter 2.0](#).

**Figure 16. DQ/DM - Data Routing Topology for a Single Rank 4L Fly-by Design - PCB Type 3**

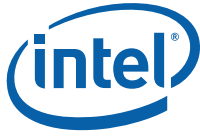


**Figure 17. DQS - Data Strobes Routing Topology for a Single Rank 4L Fly-by Design - PCB Type 3**



**Table 8. DQ/DQS Routing Guidelines and Settings for a Single Rank 4L Fly-by Design—PCB Type 3 (Sheet 1 of 2)**

Parameter	Routing Guideline / Setting		
	TL1	TL2	TL3
Transmission Line Segment	TL1	TL2	TL3
Stackup Layer (Microstrip / Stripline/ Dual Stripline)	MS	MS	MS
Characteristic Impedance (DQ/DM)	40 Ω SE 10% (MS)		
Characteristic Impedance (DQS)	76 Ω DIFF 10% (MS)		
Trace Width (W)	4.0 mils (SE) 4.0 mils (DIFF)	6.5 mils (SE) 5.3 mils (DIFF)	4.0 mils (SE) 4.0 mils (DIFF)
Trace Spacing (S1): Between DQ/DM within a data byte	min = 4.0 mils	min = 13.0 mils	min = 4.0 mils



**Table 8. DQ/DQS Routing Guidelines and Settings for a Single Rank 4L Fly-by Design—PCB Type 3 (Sheet 2 of 2)**

Parameter	Routing Guideline / Setting		
Trace Spacing (S2): Between adjacent data bytes' signals of a channel	min = 10.0 mils	min = 20 mils	min = 10.0 mils
Trace Spacing (S3): Between DQS and DQS# pair	4.0 mils	4.7 mils	4.0 mils
Trace Spacing (S4): Between DQS/DSQ# and DQ/DM	min = 4.0 mils	min = 13 mils	min = 4.0 mils
Trace Spacing (S5): Between DQ/DM/DQS group and other DDR group's signals	min = 4.0 mils	min = 13 mils	min = 4.0 mils
Trace Spacing (S6): Between DQ/DM/DQS group and other non-DDR signals - excluding power pins	min = 10.0 mils	min = 25 mils	min = 10.0 mils
DQ/DQS Trace Segment Length	max = 300 mils	min = 500 mils max = 2000 mils	max = 300 mils
DQ/DQS Total trace length	TL1 + TL2 + TL3 = <b>2600 mils (max)</b>		
Length matching between DQ/DM and DQ/DM within a Byte group (including pkg. length)	± 5 mils <b>Note:</b> All DM/DQ signals length for a given Byte Group must fall within 10 mils window.		
Length matching between DQ/DM and DQS/DQS# of a byte (including pkg. length)	DQ = (DQ/DQS# ± 5 mils)		
Length matching between Clock and DQS/DQS# (including pkg. length)	DQS = (CLK/CLK# - 1.75") ± 0.75"		
Length matching between DQS and DQS# (including pkg. length)	± 5 mils		
Number of vias	max = 2 via		
SoC Buffer Settings:	RON: 32 Ω SR: 4V/ns		
SoC Read ODT:	180 Ω		
DRAM Buffer Settings:	RON: 34 Ω		
DRAM Runtime:	120 Ω		
DRAM Ritter:	dynamic ODT not used		

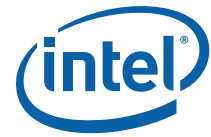


Figure 18. ODT/CKE/CS - Control Routing Topology for a Single Rank 4L Fly-by Design - PCB Type 3

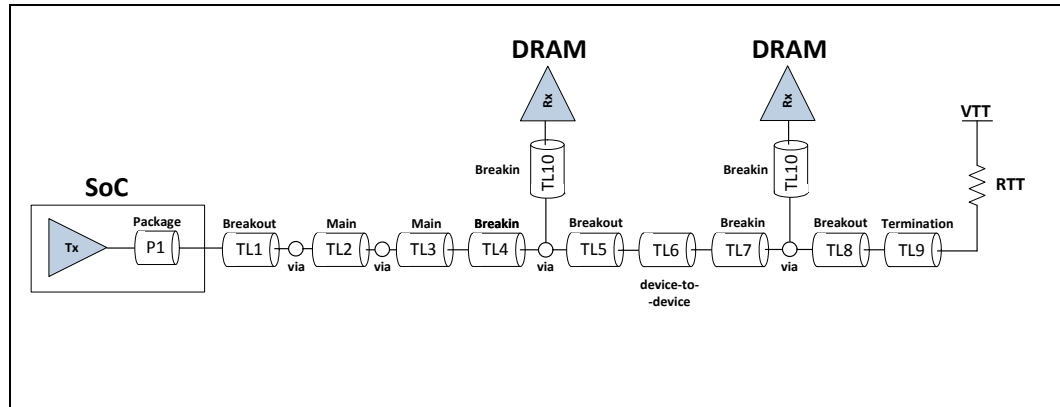


Table 9. Control - Routing Guidelines and Settings for a Single Rank 4L Fly-by Design—PCB Type 3 (Sheet 1 of 2)

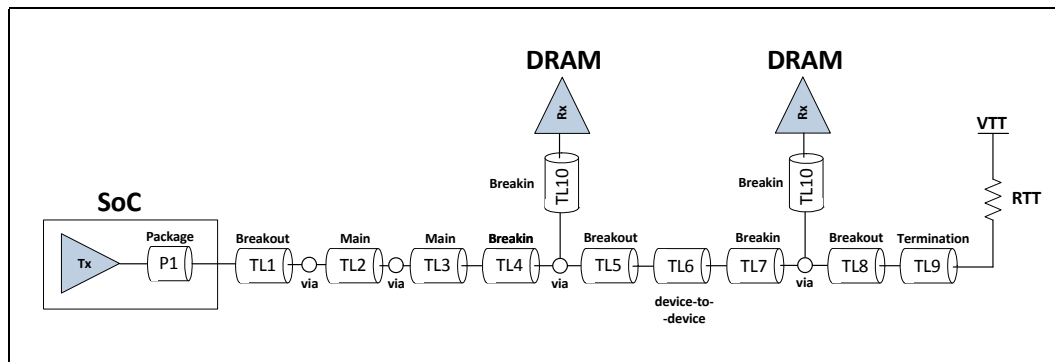
Parameter	Routing Guideline / Setting									
Transmission Line Segment	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10
Stackup Layer (Microstrip / Stripline/ Dual Stripline)	MS	MS	MS	MS	MS	MS	MS	MS	MS	MS
Characteristic Impedance (Control Group)	50 Ω SE 10% (MS)									
Trace Width	4.0 mils	4.2 mils	4.2 mils	4.2 mils	4.2 mils	4.2 mils	4.2 mils	4.2 mils	4.2 mils	4.2 mils
Trace Spacing (S): Within the signals in the point-to-point CTRL Group	min = 4.0 mils	min = 8.4 mils	min = 6.5 mils	min = 4.2 mils	min = 4.0 mils	min = 4.2 mils	min = 4.0 mils	min = 4.2 mils	min = 4.2 mils	min = 4.0 mils
Trace Spacing (S1): Between CTRL Signals and other DDR signals	min = 4.0 mils	min = 13 mils	min = 6.5 mils	min = 4.2 mils	min = 4.0 mils	min = 6.5 mils	min = 4.0 mils	min = 4.2 mils	min = 4.2 mils	min = 4.0 mils
Trace Spacing (S2): Between CTRL group and non-DDR signals - excluding power pins	min = 10.0 mils	min = 20 mils	min = 20 mils	min = 20 mils	min = 10.0 mils	min = 20 mils	min = 10.0 mils	min = 20 mils	min = 10.0 mils	min = 10.0 mils
Point-to-point CTRL group Trace Segment Length	max = 200 mils	min = 1000 mils max = 1700 mils	min = 200 mils max = 400 mils	min = 200 mils max = 600 mils	max = 100 mils	min = 500 mils max = 600 mils	max = 100 mils	min = 300 mils max = 700 mils	max = 50 mils	max = 100 mils
Point-to-point CTRL group Total trace length	1st DRAM: TL1 + TL2 + TL3 + TL4 + TL10 = 3000 mils (max) 2nd DRAM: TL1 + TL2 + TL3 + TL4 + TL5 + TL6 + TL7 + TL10 = 3800 mils (max)									

**Table 9. Control - Routing Guidelines and Settings for a Single Rank 4L Fly-by Design—PCB Type 3 (Sheet 2 of 2)**

Parameter	Routing Guideline / Setting
Length matching between point-to-point CTRL signals and all the CLOCKS within a Channel (including pkg. length)	CTRL = (CLK/CLK# - 50 mils) ± 50 mils
Number of vias	max = 4 via
SoC Buffer Settings:	RON: 27 Ω SR: 1.5 V/ns
RTT Value	36 Ω ± 10%

*Note:* All length matching and total trace length rules are applicable for the SoC to DRAM paths; for termination related segments i.e., TL8 and TL9 only the min and max trace segment length rules apply.

**Figure 19. MA/BS/CAS/RAS/ WE - Command Routing Topology for a Single Rank 4L Fly-by Design—PCB Type 3**



**Table 10. Command Routing Guidelines and Settings for a Single Rank 4L Fly-by Design—PCB Type 3 (Sheet 1 of 2)**

Parameter	Routing Guideline / Setting									
Transmission Line Segment	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10
Stackup Layer (Microstrip / Stripline/ Dual Stripline)	MS	MS	MS	MS	MS	MS	MS	MS	MS	MS
Characteristic Impedance (Command Group)	40 Ω SE 10% (MS)									
Trace Width	4.0 mils	6.5 mils	6.5 mils	4.0 mils	4.0 mils	6.5 mils	4.0 mils	4.0 mils	6.5 mils	4.2 mils
Trace Spacing (S): Within the signals in the Command Group	min = 4.0 mils	min = 13.0 mils	min = 6.5 mils	min = 4.0 mils	min = 4.0 mils	min = 6.5 mils	min = 4.0 mils	min = 4.0 mils	min = 6.5 mils	min = 4.0 mils

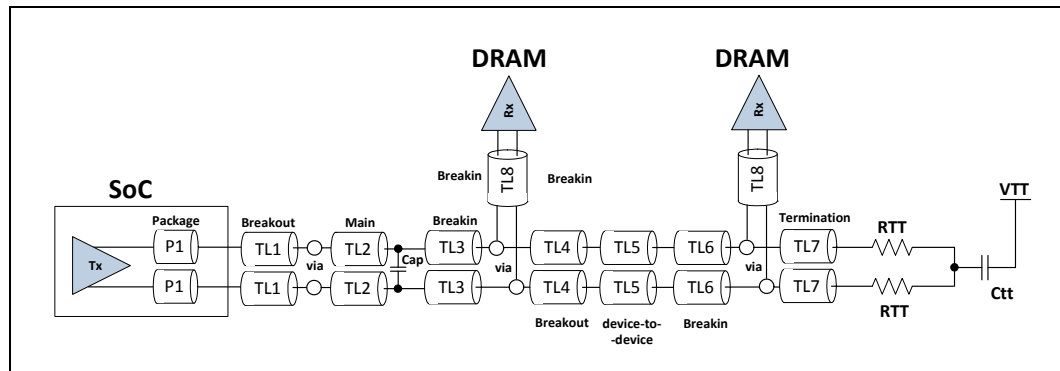


**Table 10. Command Routing Guidelines and Settings for a Single Rank 4L Fly-by Design—PCB Type 3 (Sheet 2 of 2)**

Parameter	Routing Guideline / Setting									
Trace Spacing (S1): Between Command Signals and the other DDR groups	min = 4 mils	min = 13.0 mils	min = 6.5 mils	min = 4 mils	min = 4 mils	min = 6.5 mils	min = 4 mils	min = 4 mils	min = 6.5 mils	min = 4 mils
Trace Spacing (S2): Between CMD group and non-DDR signals - excluding power pins	min = 12 mils	min = 25.0 mils	min = 25.0 mils	min = 12 mils	min = 12 mils	min = 25.0 mils	min = 12 mils	min = 12 mils	min = 25.0 mils	min = 12 mils
CMD group Trace Segment Length	max = 300 mils	min = 500 mils max = 1700 mils	min = 100 mils max = 750 mils	max = 100 mils	max = 100 mils	min = 200 mils max = 450 mils	max = 100 mils	max = 100 mils	min = 50 mils max = 600 mils	min = 50 mils max = 300 mils
CMD group Total trace length	1st DRAM: TL1 + TL2 + TL3 + TL4 + TL10 = 3150 mils (max) 2nd DRAM: TL1 + TL2 + TL3 + TL4 + TL5 + TL6 + TL7 + TL10 = 3800 mils (max)									
Length matching between CMD signals and all the CLOCKS within a Channel (including pkg. length)	CMD = CLK/CLK# ± 150 mils									
Number of vias	max = 4 via									
RTT Value	36 Ω ± 10%									
SoC BUffer Settings	RON: 27 Ω SR: 1.5 V/ns									
CMD Timings	2N									

*Note:* All length matching and total trace length rules are applicable for the SoC to DRAM paths; for Termination Segments (TL8 + TL9) only the min and max trace segment length rules apply.

**Figure 20. Clock Routing Topology for a Single Rank 4L Fly-by Design—PCB Type 3**





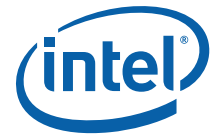
**Table 11. Clock Routing Guidelines and settings for a Single Rank 4L Fly-by Design—PCB Type 3**

Parameter	Routing Guideline / Setting							
Transmission Line Segment	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8
Stackup Layer (Microstrip / Stripline/ Dual Stripline)	MS	MS	MS	MS	MS	MS	MS	MS
Characteristic Impedance (CLK Group)	66 Ω DIFF 10% (MS)							
Trace Width	4.0 mils	7.2 mils	4.0 mils	4.0 mils	7.2 mils	4.0 mils	7.2 mils	4.0 mils
Trace Spacing (S): Between P and N of a CLK pair	4.0 mils	5.3 mils	4.0 mils	4.0 mils	5.3 mils	4.0 mils	5.3 mils	4.0 mils
Trace Spacing (S1): Between point-to-point CLK pair to another CLK pair	min = 12.0 mils	min = 25 mils	min = 4 mils	min = 4.0 mils	min = 25 mils	min = 4.0 mils	min = 25 mils	min = 4.0 mils
Trace Spacing (S2): Between point-to-point CLK Group and other DDR groups	min = 4 mils	min = 25 mils	min = 4.0 mils	min = 4.0 mils	min = 10 mils	min = 4.0 mils	min = 25 mils	min = 4.0 mils
Trace Spacing (S3): Between point-to-point CLK Group non-DDR signals	min = 4 mils	min = 25 mils	min = 12.0 mils	min = 12 mils	min = 25 mils	min = 12 mils	min = 25 mils	min = 4.0 mils
Point-to-point CLOCK group Trace Segment Length	max = 200 mils	min = 500 mils max = 2500 mils	max = 100 mils	max = 100 mils	min = 400 mils max = 600 mils	max = 100 mils	max = 450 mils	max = 200 mils
Point-to-point CLOCK group Total trace length	1st DRAM: TL1 + TL2 + TL3 + TL6 = 3000 mils (max) 2nd DRAM: TL1 + TL2 + TL3 + TL4 + TL6 = 3800 mils (max)							
Length matching between P and N of CLOCK (including pkg. length)	± 5 mils							
Number of vias	max = 3 via							
RTT Value	30 Ω ±10%							
Cap Value	1 pF							
Ctt Value	0.1 μF							
SoC Buffer Settings:	RON: 26 Ω. SR: 4V/ns							

*Note:* All length matching and total trace length rules are applicable for the SoC to DRAM paths; for Termination Segment (TL7) only the min and max trace segment length rules apply.

### 3.3.2 Memory Stackup Guidelines

Refer see [Chapter 2.0](#) for motherboard stack up details.



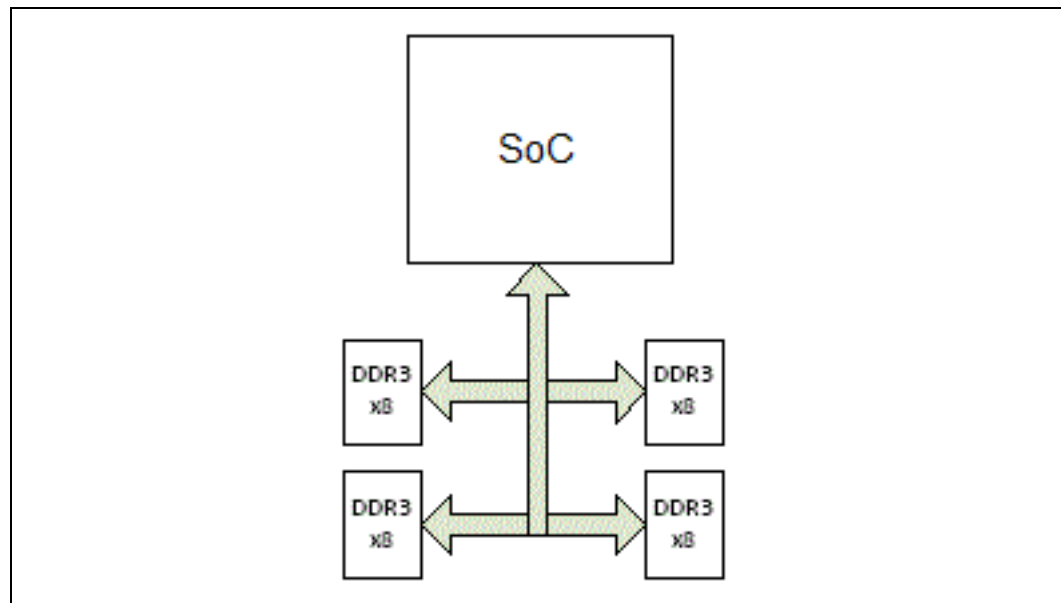
### 3.3.3 Memory Configurations and Connectivity

Figure 21 shows the DDR3 Memory Down design high level block diagram and memory channel connectivity.

#### 3.3.3.1 ODT Signal Connectivity and Support

For DDR3 memory-down design, Intel recommends ODT signals to be routed between SoC and DRAM devices on platform. This way, ODT timings at DRAM device can be fully controlled by the SoC.

Figure 21. DDR3 Memory Down Block Diagram



### 3.3.4 Memory Physical Layout Guidelines

#### 3.3.4.1 General Routing Guidelines

*Note:* For DDR3 memory down configuration, one CLK pair per rank is needed.

Here are some general DDR3 memory signal group routing guidelines:

- Recommend all of the signals to have GND referencing planes.
- Make sure proper GND stitching in place when signal is making layer transitions.
- Avoid parallel routing between two adjacent layers.
- Tuning length between Differential pairs at the DRAM devices side (some DQS/CLK will have P & N length mismatch)

#### 3.3.4.2 Byte Lane Placement

- A data channel can be treated as two separate and independent byte lanes for routing.
- Byte lanes may be partitioned between internal routing layers as required to complete the route.



- Each byte lane signal set must be routed as a group on the same layer, to minimize skew within the byte lane.

### 3.3.4.3 Via Stitching and Placement

Poor stitching via could lead to significant margin loss, so it is essential to stitch reference planes for signal transition, where the reference plane change took in place.

It is highly recommended to stitch signals both within byte/group and between bytes/groups. In case of signal transition to a layer in between two reference planes, make sure the stitching via connects to the plane closest to the signal layer. In case signal transition to another routing layer, but the referencing plane still kept the same, no stitching via is required.

### 3.3.5 Memory Bit and Byte Lane Swapping

- Bits swapping is allowed within the same byte and byte swapping is allowed within the channel. Strobes must always accompany their corresponding bytes.
- **DQS/DQS# and CLK/CLK# Swapping:** is NOT allowed on either DQS/DQS# or CLK/CLK#. DQS/DQS# must be connected correctly.
- Clock swapping is not allowed.

### 3.3.6 Memory Length Matching Guidelines

*Note:* If swapping is used, the TLC must be adjusted to comply with the required length matching requirements.

Length matching within differential pairs (CLK and DQS) should be performed at the DRAM side, e.g., at the Break-in trace segment. However, no length matching is required for the SoC breakout or main routing segments.

#### 3.3.6.1 Length Matching and Length Formulas

Please refer to each individual topology guidelines.

#### 3.3.6.2 Package Length Compensation

Package length compensation is an integral part of the overall length matching process and is important within individual byte lanes, CMD and CTRL within the channel. The SoC package traces are not length-matched internally, which makes package length compensation on the motherboard extremely important. Please refer to the DDR3 Trace Length Calculator for the actual SoC in-package trace lengths.

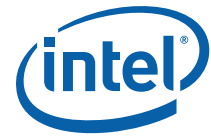
### 3.3.7 Memory Decoupling Guidelines

Refer to the *CLANTON Power Decoupling (Kips Bay) Reference* (ID# 522272).

## 3.4 Memory Reference Voltage and Compensation Guidelines

### 3.4.1 SoC DDR Reference Voltage

The Intel® Quark SoC X1000 uses an internal circuitry to adjust the reference voltage used to qualify the logic levels on incoming DDR data bits. This capability is used to perform a vertical read data eye training. The DDR\_VREF input allows supplying an external reference voltage, but in normal circumstances the internal reference voltage shall be used and DDR\_VREF input shall be connected to GND.



### 3.4.2 DRAM Reference Voltage

DRAM memory devices need to be supplied with VREF\_CA and VREF\_DQ reference voltages generated on the platform.

### 3.4.3 DRAM ZQ Calibration

The Intel® Quark SoC X1000 supports configurations with separate and shared precision resistors across DRAM devices.

In the case of separate precision resistor for each DRAM device, the ZQ Calibration is performed in parallel on all DRAM devices. This is the most straightforward configuration and is recommended for Intel® Quark SoC X1000 platforms.

To save on the BOM cost in the dual rank configuration it is also valid to share precision resistors between the ranks. In this case the ZQ calibration is performed in series - one rank at the time. The savings for Intel® Quark SoC X1000 dual rank platforms by using this approach is 4 -> 2 precision resistors with four x8 DRAM devices, and is not as significant as for the products with wider data buses and more ranks.

The precision resistor should be 240 Ohm and connected between ZQ pin and GND. For more details on ZQ signal and calibration refer to the *DDR3 JEDEC Specification*.

*Note:* The default mode of operation for the Intel® Quark SoC X1000 is the Parallel ZQ Calibration, and this mode is supported in Intel® Quark SoC X1000 MRC.

### 3.4.4 Routing Guidelines for Compensation Signals

The SoC uses precision resistors connected to DDR\_XXXPU inputs to compensate the drive strength of different buffers. It is important to follow the routing guidelines as well as board level guidelines for these signals in order to get the accuracy in the compensation scheme.

Table 12 shows the values of different precision resistors that need to be connected to the compensation pins.

*Note:* The SoC breakout area width and spacing can be reduced to 4 mils, but care needs to be taken to not route any high frequency signals next to the compensation signals.

**Table 12. Precision Resistor Value for DDR\_XXXPU Compensation Inputs**

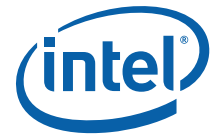
Signal	Max Via Count	Trace Width	Isolation Spacing	Resistor Value (Pull Down to GND)	Max Length
DDR3_ODTPU	2	5 mils	10 mils (to any signal)	274 Ω ±1%	1000 mils
DDR3_DQPU	2	5 mils	10 mils (to any signal)	34 Ω ±1%	1000 mils
DDR3_CMDPU	2	5 mils	10 mils (to any signal)	32.4 Ω ±1%	1000 mils

## 3.5 DataMask Guidelines

The Intel® Quark SoC X1000 does make use of the Data Mask (DM) signals. Therefore, each DM signal should connect to the appropriate memory device.

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## 4.0 PCI Express\* Design Guidelines

### 4.1 PCIe\* General Introduction

#### 4.1.1 Description

The Intel® Quark SoC X1000 SoC provides two PCI Express\* root ports. The PCIe\* root ports consist of one lane each configured as a 2x1 port. Each Root Port is PCIe\* 2.0 compliant.

**Table 13. PCI Express\* Root Ports Speed Support**

Speed	Bandwidth	Direction
PCIe* 1.0	2.5 GT/s	Each Direction (5 GT/s concurrent)

The PCI Express\* topology consists of a transmitter (TX) on one device connected by a differential trace pair to a receiver (RX) on a second device. One of the devices may be located on the baseboard or an add-in card.

#### 4.1.2 Supported Configuration Options for PCIe\* Ports

Table 14 describes the supported configurations for the PCIe ports.

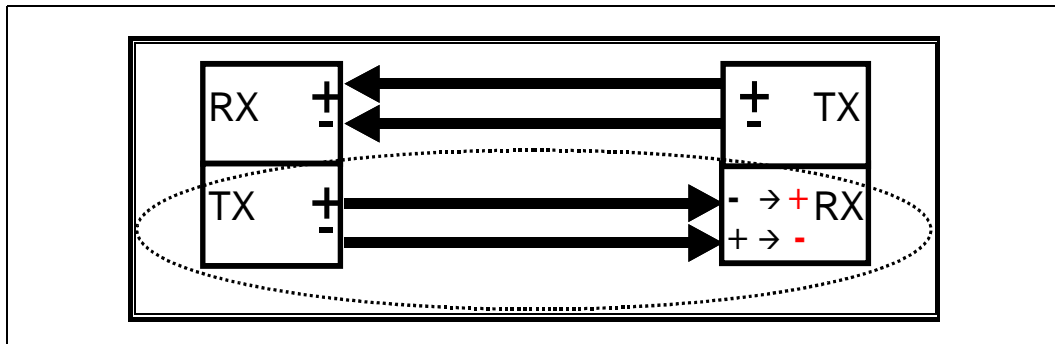
**Table 14. PCIe\* Root Ports 1 and 2 Supported Configurations**

Port 1	Port 2	Notes
x1	x1	2x1 mode, one lane to each port

#### 4.1.3 PCI Express\* Lane Polarity Inversion

The PCI Express\* Base Spec requires polarity inversion to be supported independently by all **receivers** across the Link - each differential pair within each Lane of the PCIe Link handles its own polarity inversion. Polarity inversion is applied, as needed, during the initial training sequence of the Lane. In other words, a Lane will still function correctly even if a positive (TX+) signal from a transmitter is connected to the negative (RX-) signal of the receiver. Polarity inversion eliminates the need to untangle a trace route to reverse a signal polarity difference within a differential pair and no special configuration settings are necessary in the SoC to enable it. It is important to note that polarity inversion does not imply direction inversion or direction reversal, i.e., the TX differential pair from one device must still connect to the RX differential pair on the receiving device, per the PCIe Base Spec. Polarity Inversion is not the same as "PCI Express\* Port Lane Reversal". See Figure 22 for an example.

Figure 22. Polarity Inversion on a TX to RX Interconnect



#### 4.1.4 PCI Express\* Port Lane Reversal

As each PCIe port link is a single lane, Lane Reversal is not supported in SoC.

#### 4.1.5 PCIe\* Port Disabling Guidelines

- If some of the PCI Express ports are not implemented on the platform:
  - PETp/n [x] and PERp/n [x] signals may be left unconnected, where 'x' is the port number left as no connect.
- If no PCI Express ports are implemented on the platform:
  - PETp/n [8:1] and PERp/n [8:1] may be left unconnected.

*Note:* Pull-up Wake# to S# 3.3V power well via an on-platform 10-kΩ resistor. Check with latest version of the *Intel® Quark SoC X1000 Datasheet* for maximum leakage specification on WAKE# pin while selecting a pull up resistor in order to ensure SOC Vih at the pin is satisfied.

#### 4.1.6 Length Matching Guidelines

The key about differential signal length-matching is that the differential signal pair components (i.e. the + and - signals) must be kept in-phase during the entire length of the traces (from beginning to end). Most board designers try to keep the overall trace length of the individual + and - differential signals matched to within 10 mils (Table 19) of each other. However, this is not sufficient - or necessarily correct. It is important to do length-matching on a per-segment basis, in order to ensure the differential signals are kept in-phase, which gives optimal differential impedance and Common Mode rejection. Further length-matching information can be found in Appendix A, "General Differential Signals Design Guidelines".

#### 4.1.7 Difference Between PCIe Ports and Lanes

A PCIe Lane is composed of a single pair of RX and TX signals (e.g., RX0+/RX0- and TX0+/TX0- make up PCIe Lane 0). A PCIe Link is composed of one or more PCIe Lanes (e.g. bundling 2 PCIe Lanes together would make a x2 PCIe Link). A PCIe Link is addressed by the lowest number PCIe Port it connects to in the SoC (e.g., a x2 PCIe Link connected to PCIe Ports 0 and 1 would be called x2 PCIe Port 0).



## 4.1.8 Impedance Compensation and Voltage Reference

The compensation input is used by the circuitry to determine, check and adjust the system buffer output strength and characteristic impedance over temperature, process and voltage variations. This is done by comparing its buffer impedance against a standard reference resistor, RCOMP.

The RCOMP signals should be referenced to VSS. Noisy or switching references should be avoided. As board space allows, it is recommended to add a VSS shield at least 4 mils wide placed between PCIE\_IRCOMP/PCIE\_RBIAS and adjacent I/O. No shield is needed between PCIE\_RBIAS and PCIE\_IRCOMP.

**Table 15. SoC PCI Express\* Compensation and Voltage Reference Guidelines**

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_IRCOMP	4.2 mils min (breakout) 12-15 mils (trace) <b>Note:</b> Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	7.5k ohm $\pm$ 1% pulled to VCC1P5_S0.	Max total= 500 mils
PCIE_RBIAS	4.2 mils min (breakout) 12-15 mils (trace) <b>Note:</b> Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	7.5k ohm $\pm$ 1% pulled to VCC1P5_S0.	Max total= 500 mils

## 4.1.9 Reference Documents

**Table 16. PCI Express\* Reference Documents**

Title	Doc#/Location
PCI Express Base Specification Rev 2.1	<a href="http://www.pcisig.com/home">http://www.pcisig.com/home</a>
PCI Express Electromechanical Specification Rev2.0	<a href="http://www.pcisig.com/home">http://www.pcisig.com/home</a>

## 4.2 PCIe\* Signal Descriptions

### 4.2.1 Signal Groups

**Table 17. PCI Express\* Signal Groups (Standard Card)**

Group	Signal Name	Description
Data	PCIE_PETP_0, PCIE_PETN_0 PCIE_PETP_1, PCIE_PETN_1	PCI Express* Transmit Differential-Pair
Data	PCIE_PERP_0, PCIE_PERN_0 PCIE_PERP_1, PCIE_PERN_1	PCI Express* Receive Differential-Pair

### 4.3 PCIe\* Topology Guidelines

Table 18. PCI Express\* Card Topologies

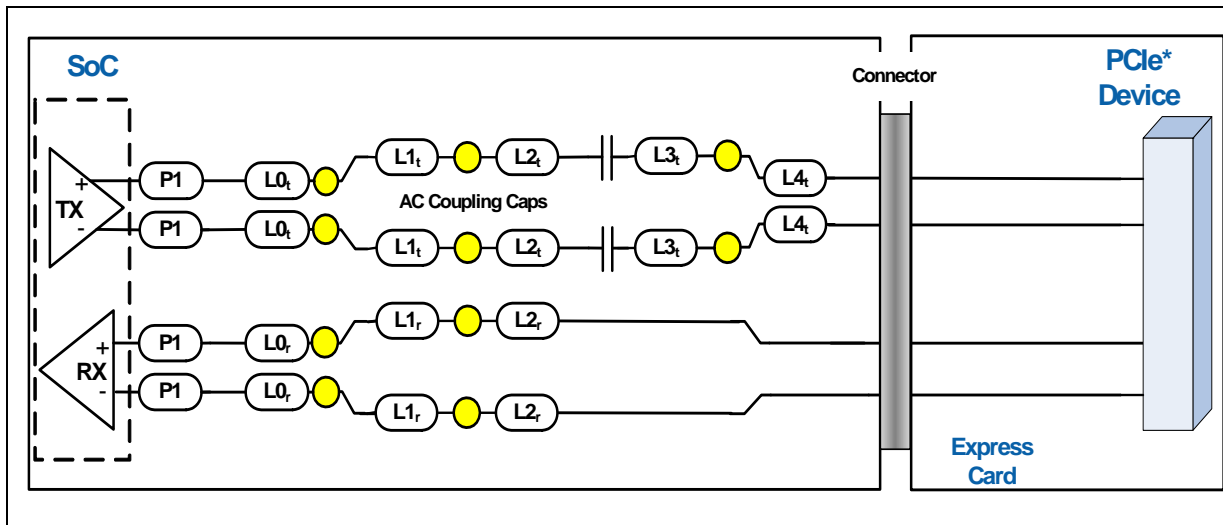
Parameter	Recommendation
Topology	Point to point with AC coupling depending on the topology.
Reference Plane	Ground

#### 4.3.1 Expansion Card Connector Topology

The Design Guide recommendations are based on surface mount connectors that meet the insertion loss and return loss characteristics as specified in PCI Express\* CEM 2.0 Specification. These guidelines include all trace routing on the board and the breakout region.

- For PCI Express\* interface composed of x1 links, it is most practical to route the TX signals and RX signals of each link next to each other on the same layer following interleaved routing.
- The PCI Express\* expansion card topology simulations showed the lowest margins compared to other PCI Express\* interfaces. Additional simulation may be required for different specific design scenarios.
- For a 4 layer board only microstrip (MS) are applicable.
- AC coupling capacitors for TX pair on the motherboard are recommended to be placed very close to the expansion connector. Avoid placing AC caps at the center of the motherboard main route.
- Refer to [Section 10.3.1](#) for PCIe\* clock guidelines.

Figure 23. PCI Express\* Expansion Card Connector Topology





**Table 19. PCI Express\* Expansion Card Routing Tx to Connector**

Transmission Line Segment	P1/L0 <sub>t</sub>	L1 <sub>t</sub>	L2 <sub>t</sub>	L3 <sub>t</sub>	L4 <sub>t</sub>
PCB Routing Layer(s) Optional	4 Layer	4 Layer	4 Layer	4 Layer	4 Layer
Stackup Layer (Microstrip / Stripline/ Dual Stripline)	MS	MS	MS	MS	MS
Characteristic Impedance	90 Ω diff 15%(MS) 90 Ω diff 15% (SL)	90 Ω diff 15%(MS) 90 Ω diff 15% (SL)	90 Ω diff 15%(MS) 90 Ω diff 15% (SL)	90 Ω diff 15%(MS) 90 Ω diff 15% (SL)	90 Ω diff 15% (MS) 90 Ω diff 15% (SL)
Trace Width (w) <sup>1</sup>	4.0 mils	4.0 mils	4.0 mils	4.0 mils	4.0 mils
Trace Spacing (S): Between P and N within a diff pair	4.0 mils	6.0 mils	6.0 mils	6.0 mils	6.0 mils
Trace Spacing(S1): Between PCIe TX/RX diff pairs <sup>2</sup>	12.0 mils	15.0 mils	15.0 mils	15.0 mils	15.0 mils
Trace Spacing(S2): Between PCIe TX diff pairs and RX diff pairs <sup>3</sup>	12.0 mils	18.0 mils	15.0 mils	15.0 mils	15.0 mils
Trace Spacing(S3): Between PCIe diff pairs and other signals <sup>4</sup>	12.0 mils	18.0 mils	15.0 mils	15.0 mils	15.0 mils
TX/ RX Trace Segment Length	max = 400 mils	min = 1500 mils max = 3000 mils	max = 200 mils	max = 200 mils	max = 200 mils

1. It may not be possible to maintain the impedance in the break-in, break-out or other pin fields. For those segments, define the minimum trace width that should be maintained in that segment considering the manufacturing reliability and skin effect losses.
2. Define the edge-to-edge space between differential pairs as multiple of the distance to the nearest continuous reference plane. For example, if the nearest reference plane is 4 mils away from the signal layer then a space of 4xh means the edge-to-edge space from one pair to the next pair is 16 mils.
3. Space rules between TX diff pairs and RX diff pairs apply to the interleaved routing when TX and RX pairs are routed in interleave mode on the same layer. It also applies to the case when TX and RX pairs are on adjacent Dual Strip Line
4. Define the edge-to-edge space between differential pairs as multiple of the distance to the nearest continuous reference plane. For example, if the nearest reference plane is 4 mils away from the signal layer then a space of 4xh means the edge-to-edge space from one pair to the next pair is 16 mils.

Total Trace Length (PCIe TX) <sup>1</sup>	TX/RX Total Length = 4000 mils
Number of vias allowed	3 via

1. Does not include in package routing

Length Matching Rules	
Length Matching between P and N within a diff. pair	+/- 10 mils
<b>General</b>	
Reference plane	Continuous Ground Only



<b>DC Blocking Cap</b>	
Capacitor Value, size	0.1 $\mu$ F
<b>Capacitor location</b>	
Place the capacitors close to slot connectors	
<b>Capacitor Placement</b>	
1.	Place the caps for P and N of a diff pair at exact same location
2.	Symmetrically route the P and N from SOC to the Cap.
3.	Symmetrically route the P and N from cap to the Connector
4.	Stagger the caps of different differential pairs

**Table 20. PCI Express\* Expansion Card Routing Rx to Connector**

Transmission Line Segment	P1/L0 <sub>r</sub>	L1 <sub>r</sub>	L2 <sub>r</sub>
<b>PCB Routing Layer(s) Optional</b>	4 Layer	4 Layer	4 Layer
<b>Stackup Layer (Microstrip / Stripline/ Dual Stripline)</b>	MS	MS	MS
<b>Characteristic Impedance</b>	90 $\Omega$ diff 15% (MS) 90 $\Omega$ diff 15% (SL)	90 $\Omega$ diff 15% (MS) 90 $\Omega$ diff 15% (SL)	90 $\Omega$ diff 15% (MS) 90 $\Omega$ diff 15% (SL)
<b>Trace Width (w)</b>	4.0 mils	4.0 mils	4.0 mils
<b>Trace Spacing (S): Between P and N within a diff pair</b>	4.0 mils	6.0 mils	6.0 mils
<b>Trace Spacing(S1): Between PCIe* TX/ RX diff pairs</b>	12.0 mils	15.0 mils	15.0 mils
<b>Trace Spacing(S2): Between PCIe* TX diff pairs and RX diff pairs</b>	12.0 mils	18.0 mils	15.0 mils
<b>Trace Spacing(S3): Between PCIe* diff pairs and other signals</b>	12.0 mils	18.0 mils	15.0 mils
<b>TX/ RX Trace Segment Length</b>	max = 400 mils	min = 1500mils max = 3000 mils	max = 200 mils

<b>Total Trace Length (PCIe* TX)</b>	TX/RX Total Length = 3600 mils
<b>Number of vias allowed</b>	2 via

<b>Length Matching Rules</b>	
Length Matching between P and N within a diff. pair	+/- 10 mils
Length matching between Tx pairs of multiple lanes	+/- 10 mils
Length matching between RX pairs of multiple lanes	+/- 10 mils
<b>General</b>	
Reference plane	Continuous Ground Only



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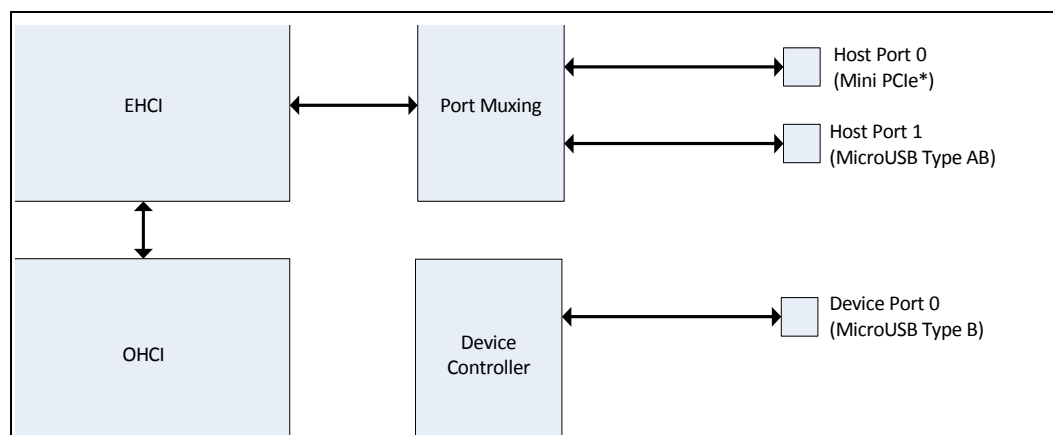
## 5.0 Universal Serial Bus 2.0 Design Guidelines

### 5.1 USB 2.0 General Introduction

#### 5.1.1 Description

The Intel® Quark SoC X1000 supports up to 2 USB 2.0 Host ports that can be used to connect to high-speed, full-speed, and low-speed USB devices via an EHCI controller and/or a OHCI USB controller. The OHCI USB controller provides USB 1.0 & 1.1 support. Additionally the SoC supports a single USB 2.0 Device port that can be used to connect to high-speed and full-speed USB devices. The SoC USB controller is also USB 1.1 capable.

Figure 24. USB Port Mapping



#### 5.1.2 Compliance Documents

Title	Doc #/Location
USB 2.0 Specification & Compliancy Requirements	<a href="http://www.usb.org">www.usb.org</a>



## 5.2 USB 2.0 Signal Descriptions

### 5.2.1 Signal Groups

Table 21. Signal Groups

Group	Signal Name	Description
DATA	USBH0_DP, USBH0_DN USBH1_DP, USBH1_DN USBD_DP, USBD_DN	Universal Serial Bus Port Differential Pairs
OVERCURRENT	USBH0_OC_B USBH1_OC_B	Overcurrent Indicators
POWER_EN	USBH0_PWR_EN USBH1_PWR_EN	Power Enables to Platform Regulators

**Note:** The connectors must meet the USB2.0 Connector Specification.

### 5.2.2 Overcurrent Protection

Intel® Quark SoC X1000 has implemented two USB overcurrent signals. The 2 overcurrent pins are connected to the two host USB 2.0 ports. Each of the OC pins needs to be connected to an external over current protection circuit, see [Figure 25](#) for an example. Each USB port may draw up to 500 mA. The overcurrent protection circuitry needs to be able to support at least 2 A to ensure proper functionality of USB compliant devices. However, if a fault device is plugged into the USB port it should trigger an overcurrent when current drawn is more than 500 mA. Designer must balance between optimum cost and protection level.

When the current rating of the protection circuit has been decided, it is crucial to ensure that the overcurrent layout is designed to support the amount of current expected. For example when the overcurrent circuit is designed to support up to 2A the overcurrent trace layout should be using a big fat trace or plane that can sustain at least 2A of current. Failure to design the trace to support high current may cause the trace on motherboard to burn out and cause permanent damage to the protection circuit. The overcurrent signals require a pull-up to the 3.3 V Suspend Rail with 8.2 kΩ to 10 kΩ resistor.

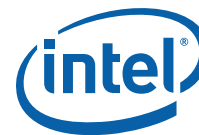
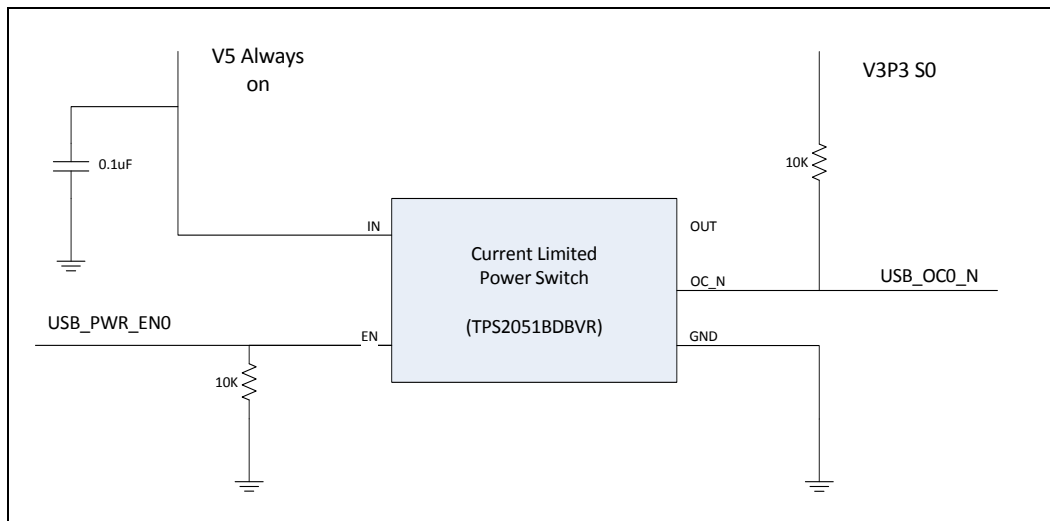


Figure 25. Sample Over Current Protection Circuit



Each overcurrent pin protects one USB port. It is system software's (BIOS) responsibility to program the overcurrent registers of the given USB controller correctly and to make sure that each USB port is protected by only one overcurrent pin. Operation with more than one overcurrent pin mapped to a port is undefined. See the *Intel® Quark SoC X1000 Datasheet* for more details.

### 5.3 USB 2.0 Topology Guidelines

#### 5.3.1 External Topologies

The external topology refers to the routing of USB signals to a microUSB connector. It is recommended that each USB data line be routed with a common mode choke and ESD protection.

Figure 26. USB 2.0 MicroUSB Topology

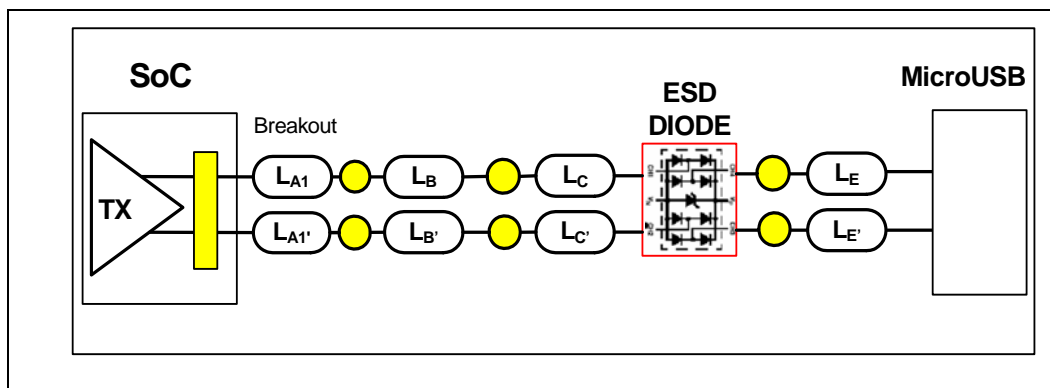




Table 22. USB 2.0 External Routing Guidelines MicroUSB

	Breakout 1			
PCB Routing Layer(s) optional	4 Layer	4 Layer	4 Layer	4 Layer
Transmission Line Segment	L <sub>A</sub>	L <sub>B</sub>	L <sub>C</sub>	L <sub>E</sub>
Routing Layer (Microstrip / Stripline / Dual Stripline)	MS	MS	MS	MS
Characteristic Impedance (Differential)	90 Ω +/- 10%	90 Ω +/- 10%	90 Ω +/- 10%	90 Ω +/- 10%
Trace Width (w)	4.0 mil	4.0 mil	4.0 mil	4.0 mil
Trace Spacing (S1): Between P and N of clock pair	4.0 mil	6.0 mil	6.0 mil	6.0 mil
Trace Spacing (S2): Between USB2 different pairs	6.0 mil	15 mil	15 mil	15 mil
Trace Spacing (S3): Between USB2 pairs and other signals	6.0 mil	25 mil	25 mil	25 mil
Trace Segment Length	0.5" max	0.1" - 2.0"	0.2" max	0.5" max

**Note:** Recommend a cable length of 9" or less for connectivity from a microUSB to panel based standard USB connector.

Length Matching Rules	
Length Matching between P and N within a diff. pair	+/- 5 mil
General	
Number of vias	max 3 vias
Routing Symmetry	Symmetrical routing of P and N of a diff pair including vias
Layer Assignment	See recommendations above
Reference plane	Ground Only
MCH Settings	Gold_cie69_usb2_tx_drv_hspice_rev1p0_ww28
	vswing = 0.42
	Preemp = 0.19054 (40mV)



Figure 27. USB 2.0 Mini PCIe Topology

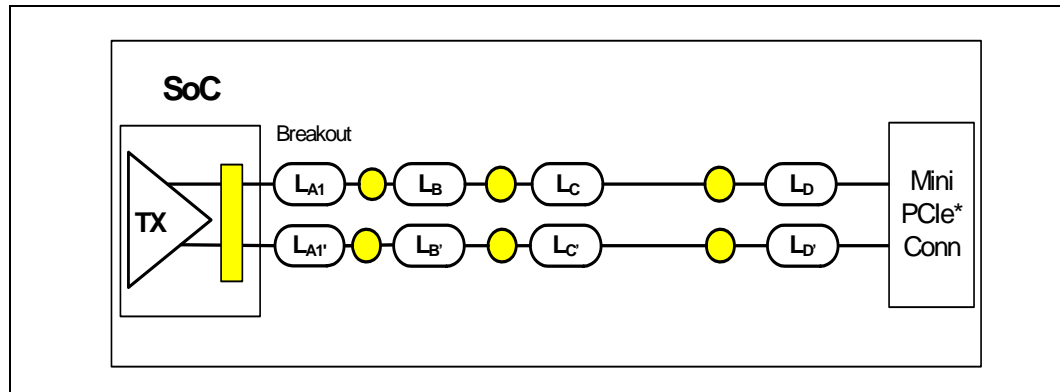


Table 23. USB 2.0 External Routing Guidelines Mini PCIe\*

	Breakout			
PCB Routing Layer(s) Optional	Routing Layer TBD	Routing Layer TBD	Routing Layer TBD	Routing Layer TBD
Transmission Line Segment	LA	LB	LC	LD
Routing Layer (Microstrip / Stripline / Dual Stripline)	MS	MS	MS	MS
Characteristic Impedance (Differential)	90 Ω +/- 10%	90 Ω +/- 10%	90 Ω +/- 10%	90 Ω +/- 10%
Trace Width (w)	4.0 mil	4.0 mil	4.0 mil	4.0 mil
Trace Spacing (S1): Between P and N of clock pair	4.0 mil	6.0 mil	6.0 mil	6.0 mil
Trace Spacing (S2): Between USB2 different pairs	6.0 mil	15 mil	15 mil	15 mil
Trace Spacing (S3): Between USB2 pairs and other signals	6.0 mil	25 mil	25 mil	25 mil
Trace Segment Length	0.5" max	0.1" - 2.0"	0.2" max	0.5" max

Note: Can support up to 2" on the Mini PCIe Card

Length Matching Rules	
Length Matching between P and N within a diff. pair	+/- 5 mil
<b>General</b>	
Number of vias	max 3 vias
Routing Symmetry	Symmetrical routing of P and N of a diff pair including vias
Layer Assignment	See recommendations above
Reference plane	Ground Only



MCH Settings	Gold_coe69_usb2_tx_drv_hspice_rev1p0_ww28
	vswing = 0.42
	Preemp = 0.09527 (20mV)

### 5.3.2 USB Connector Recommendations

Proper connector choice is critical to ensure adequate USB signal quality. For the Intel® Quark SoC X1000 the initial recommendation is the use of single USB connectors, empirical data has shown that quad-stack USB and DisplayPort\*/USB stack connectors may add interference causing poor USB signal quality. Refer to [usb.org](http://usb.org) for a list of tested connectors.

#### 5.3.2.1 External Connector Recommendations

The cable and PCB mating connector must pass the TDR requirements listed in the USB 2.0 Specification

##### 5.3.2.1.1 USB 2.0 Internal Connector

It is possible to define the internal connector pin list based on individual needs. However, an example connector pin list for 2-port internal cable connection supporting USB 2.0 is shown below.

*Note:* The Intel® Quark SoC X1000 does not support USB 3.0



**Figure 28. Example of Internal Connector Pin Assignment and Description**

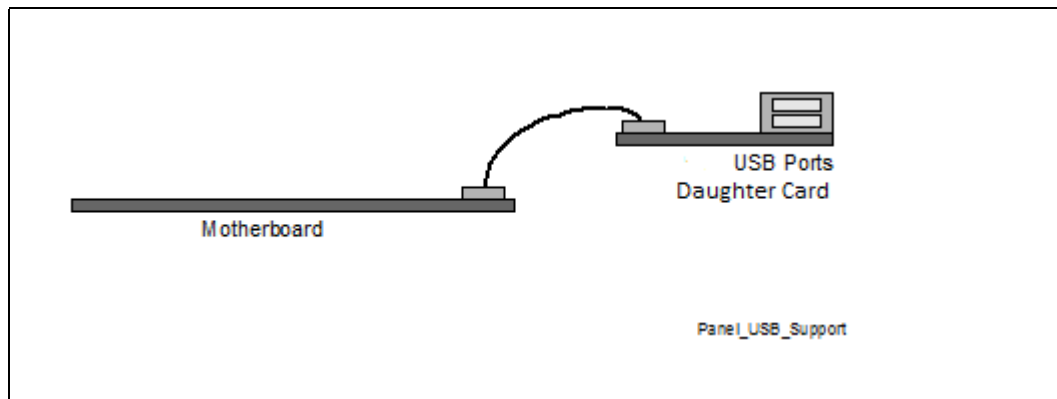
Pin No.	Signal	Description
1	RSVD	Reserved Pin
2	Vbus	5V bus Power
3	Vbus	5V bus Power
4	Vbus	5V bus Power
5	USB2_D0P	USB2 Port0 D-
6	USB2_D0N	USB2 Port0 D+
7	PWR_GND	Power GND return
8	USB_D1P	USB2 Port1 D-
9	USB_D1N	USB2 Port1 D+
10	PWR_GND	Power GND return
11	RSVD	Reserved Pin
12	RSVD	Reserved Pin
13	SIG_GND	Signal GND return
14	RSVD	Reserved Pin
15	RSVD	Reserved Pin
16	SIG_GND	Signal GND return
17	RSVD	Reserved Pin
18	RSVD	Reserved Pin
19	SIG_GND	Signal GND return
20	RSVD	Reserved Pin
21	RSVD	Reserved Pin
22	SIG_GND	Signal GND return

### 5.3.3 Daughter Card

The best way to provide internal support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. [Figure 29](#) shows the major components associated with a typical USB solution that uses a daughter card.

When designing the motherboard with internal topology support, the system integrator should know which type of cable assembly will be used. If the system integrator plans to use a connector card, ensure that there aren't duplicate EMI/ESD/thermistor components placed on the motherboard, as this will usually cause drop/droop and signal quality degradation or failure.

Figure 29. Daughter Card



### 5.3.3.1 Daughter Card Design Guidelines

The following are recommended when designing a USB 2.0 daughter card:

- Place the VBUS bypass capacitor, CMC, and ESD suppression components on the daughter card as close as possible to the connector pins.
- Follow the same layout, routing and impedance control guidelines as specified for motherboards.
- Use the same mating connector pinout as - USB 2.0 Internal Connector Pinout (Motherboard).
- Minimize the trace length on the daughter card - Less than a 2-inch trace length is recommended.
- Use the same routing guidelines as described in USB 2.0 Stackup Guidelines.
- Power and ground nets should have double vias. Trace lengths should be kept as short as possible.

## 5.4 USB 2.0 Stackup Guidelines

### 5.4.1 Stackup and Layer Utilization Guidelines

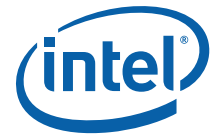
Please see the 4 Layer Stackup Chapters for all IO routing guidelines including USB 2.0.

## 5.5 USB 2.0 Configuration, Connectivity, Block Diagram

### 5.5.1 Port Power Delivery

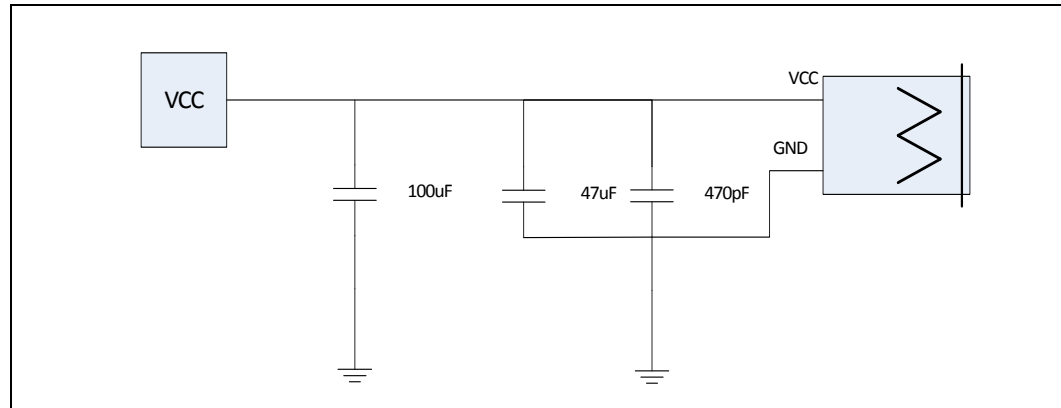
The following is a suggested topology for power distribution of VBUS to USB ports. These circuits provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach flyback protection. These two types require both bulk capacitance (droop) and filtering capacitance (for dynamic detach flyback voltage filtering). Intel recommends the following:

- Minimize the inductance and resistance between the coupling capacitors and the USB ports.
- Place capacitors close as possible to the port and the power-carrying traces should be as wide as possible, preferably, a plane.



- Make the power-carrying traces wide enough that the system fuse blows on an overcurrent event. If the system fuse is rated at 1 A, then the power-carrying traces should be wide enough to carry at least 1.5 A.

### Good Downstream Power Connection



## 5.6 USB 2.0 Length Matching Guidelines

### 5.6.1 Length Matching and Length Formulas

Please refer to the General Differential Design Guide in [Appendix A](#) for length matching guidelines.

## 5.7 USB 2.0 Additional Guidelines

### 5.7.1 EMI and ESD Protection

Please refer to [Chapter 17.0, "Electromagnetic Interference"](#) and [Chapter 18.0, "Electrostatic Discharge \(ESD\)"](#).

## 5.8 USB 2.0 Disabling and Termination Guidelines

If a USB port(s) is not implemented on the platform:

- USB P/N [x] signals can be left unconnected

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## 6.0 I<sup>2</sup>C\* Interface Design Guidelines

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### 6.1 I<sup>2</sup>C\* General Introduction

#### 6.1.1 Description

There is a single I<sup>2</sup>C\* controller in Intel® Quark SoC X1000. The interface is a two-wire I<sup>2</sup>C serial interface consisting of a serial data line and a serial clock, only 3.3v operation is supported. The I<sup>2</sup>C interfaces are intended to support various sensors on the platform.

Each I<sup>2</sup>C interface supports standard mode (up to 100 Kb/s) and fast mode (up to 400 Kb/s).Fast mode plus (up to 1 Mb/s) and High speed mode (up to 3.4 Mb/s) are not supported.

#### 6.1.2 Reference Specifications

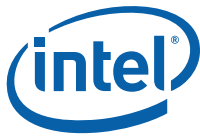
Title
I <sup>2</sup> C Specification Version 2.1

### 6.2 I<sup>2</sup>C\* Signal Descriptions

#### 6.2.1 Signal Groups

Table 24. I<sup>2</sup>C Signals

Group	Signal Name	Description
Clock	I2C_CLK	I <sup>2</sup> C Clock signal
Data	I2C_DATA	I <sup>2</sup> C Data signal



## 6.3 I<sup>2</sup>C\* Topology Guidelines

### 6.3.1 General Design Considerations

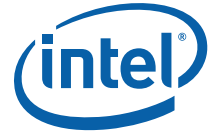
- I<sup>2</sup>C clock and data signals require pull-up resistors. The pull-up resistor size is dependent on the bus capacitive load (this includes all device leakage currents). The maximum bus capacitive load for each I<sup>2</sup>C bus is 400 pF. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the I<sup>2</sup>C rise and fall time specification. Refer to Table 27 for recommendations on pull-up resistors depending on bus capacitance.
- Do not mix and match devices supporting 100 KHz/400 KHz speed with the one supporting 1 MHz on the same I<sup>2</sup>C bus.

### 6.3.2 Detailed Routing Requirements

Table below shows detailed routing requirement for I<sup>2</sup>C bus. Note that, since I<sup>2</sup>C trace length is dependent on total capacitance of the bus, designer needs to take into consideration the number and types of I<sup>2</sup>C devices on each I<sup>2</sup>C bus. Refer to Table 26 for guidance on trace capacitance.

Table 25. I<sup>2</sup>C\* Signal Routing Summary

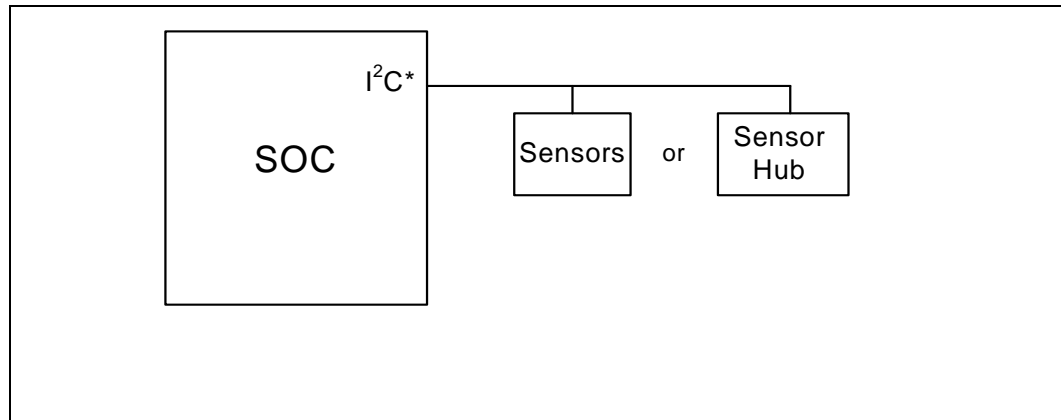
Parameter	Stackup	Units	Routing Recommendation	
			I <sup>2</sup> C_DATA	I <sup>2</sup> C_CLK
Trace Width	MS	mils	4	4
Trace Spacing	MS	mils	5	15
Breakout width	MS	mils	3.5	
Breakout Spacing	MS	mils	4	
Max Breakout Length	NA	mils	500	500
Length Matching	NA	mils	540	
Impedance	MS	ohm	50Ω ±10%	50Ω ±15%

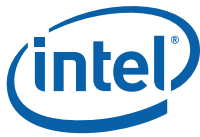


## 6.4 I<sup>2</sup>C\* Connectivity

The I<sup>2</sup>C interface is primarily to support various sensors which may have different bandwidth requirements on the platform. As devices supporting 100 Kb/s and/or 400 Kb/s cannot be mixed on the same I<sup>2</sup>C bus with higher speed devices, system designer must consider what types of devices, taking into account of their required bandwidth, to determine connectivity on the I<sup>2</sup>C bus.

Figure 30. Example of Devices on I<sup>2</sup>C\* Bus





## 6.5 I<sup>2</sup>C\* Additional Guidelines

System designers must consider the total bus capacitance, which includes both MCP and device pin capacitance and board trace length capacitance when designing I<sup>2</sup>C bus. The total bus capacitance must not exceed 400 pF. Table 26 and Table 27 below provide info to help determine total bus capacitance and proper pull-up resistors on the I<sup>2</sup>C buses. Analysis of a particular layout is still required to confirm correct operation.

Table 26. Bus Capacitance Reference Chart

Device	Capacitance Includes	Units	Capacitance
MCP	Pin Capacitance	pF	10
Board Trace per Inch	TBD pF per inch of trace length	pF	TBD

Table 27. Example Bus Capacitance/Pull-Up Resistor Relationship

Physical Bus Segment Capacitance	Pull-Up Range (For V <sub>CC</sub> = 3.3 V) 100kHz	Pull-Up Range (For V <sub>CC</sub> = 3.3 V) 400kHz
10 to 50 pF	NA	NA
50 to 100 pF	NA	NA
10 to 100 pF	9 kΩ to 1 kΩ	2.4kΩ to 0.4 kΩ
100 to 200 pF	5 kΩ to 1 kΩ	1.6 kΩ to 0.4 kΩ
200 to 300 pF	3.5 kΩ to 1 kΩ	1 kΩ to 0.4 kΩ
300 to 400 pF	2.5 kΩ to 1 kΩ	0.8 kΩ to 0.4 kΩ

## 6.6 Terminating Unused I<sup>2</sup>C Signals

If I<sup>2</sup>C interfaces are not used, the signals should be terminated properly with external pull-up or pull-down resistors.

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## 7.0 SDIO Interface Design Guidelines

### 7.1 SDIO General Introduction

#### 7.1.1 Description

Intel® Quark SoC X1000 implements a single SDIO interface that is only intended for general-purpose connections, such as SD cards. It supports SDIO card specification 3.0 and the MMC specification 3.31, 4.2, and 4.41. Support for up to 400 Mbits/s operation using 8-bit parallel lines (MMC8 mode) and 200 Mbits/s using 4 parallel lines (sd4 mode).

The physical connection supports the dynamic removal/insertion of cards by end users.

### 7.2 SDIO Signal Descriptions

#### 7.2.1 Signal Groups

**Table 28. SDIO Signals**

Group	Signal Name	Description
Clock	SD_CLK	SDIO Clock signal
Data	SD_DATA_0, SD_DATA_1,SD_DATA_2, SD_DATA_3,SD_DATA_4, SD_DATA_5,SD_DATA_6, SD_DATA_7	SDIO Data signals
Command	SD_CMD SD_WP SD_LED	SDIO Command Signal
Power Enable	SD_PWR_B	Output from the MCP for controlling device power

### 7.3 SDIO Topology Guidelines

This section contains preliminary information and details for layout and routing guidelines for the SDIO interfaces.

Figure 31. SDIO Topology with Connector

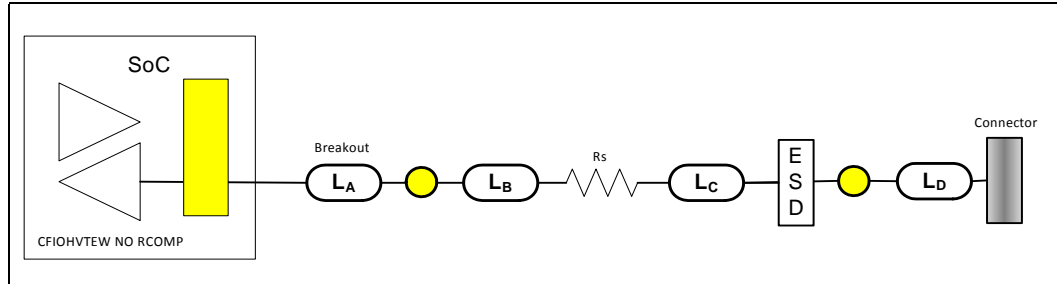


Table 29. SDIO Layout Guideline

	Breakout			
PCB Routing Layer(s) Optional	4 Layer	4 Layer	4 Layer	4 Layer
Transmission Line Segment	$L_A$	$L_B$	$L_C$	$L_D$
Routing Layer (Microstrip / Stripline / Dual Stripline)	MS	MS	MS	MS
Characteristic Impedance (Single-ended)	50 $\Omega$ +/- 15%	50 $\Omega$ +/- 10%	50 $\Omega$ +/- 10%	50 $\Omega$ +/- 10%
Trace Width (w)	4.2 mil	4.2 mil	4.2 mil	4.2 mil
Trace Spacing(S2): Between SDIO Signals	4.2 mil	10 mil	10 mil	4.2 mil
Trace Spacing(S3): Between SDIO and other signals	4.2 mil	10 mil	10 mil	4.2 mil
Trace Segment Length	0.5" max	0.1" - 0.8"	0.1" - 3.0"	0.5" max

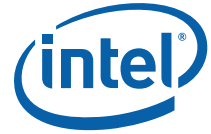
**Note:** \* Keep  $L_A + L_B$  as short as possible to give the best margin on the overshoot/undershoot violation.

Data to Clock MB length matching rule <sup>1</sup>	< 200mils
Number of vias	max 2
$R_S$	33 $\Omega$ +/- 5%
Reference Plane	Solid Ground Reference

1. Relates to platform routing, inter-package routing not considered.

### 7.4 Terminating Unused SDIO Signals

If SDIO interface is not used, it should be terminated properly with external pull-up or pull-down resistors. See Table 30 regarding internal pull up/down.


**Table 30. SOC SDIO Pull Up/Down**

Pin	Status
SD_CLK	External Weak Pull Up or Pull Down as appropriate for strapping
SD_DATA_0, SD_DATA_1,SD_DATA_2, SD_DATA_3,SD_DATA_4, SD_DATA_5,SD_DATA_6, SD_DATA_7	Internal 20K Pull Up
SD_CMD	Internal 20K Pull Up
SD_PWR_B	External Weak Pull
SD_WP	Internal 20K Pull Down
SD_LED	No internal Pull Up or Pull Down

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## 8.0 UART Interface Design Guidelines

### 8.1 General Introduction

#### 8.1.1 Description

The Intel® Quark SoC X1000 SoC integrates two UART controllers. Each supports up to a max 2.76 Mbit/s. The interfaces support 3.3V only. The controllers can be used in the low-speed, full-speed, and high-speed modes. The UART controllers are based on the 16550 industry standard. The UART interfaces can be utilized to support various sensors or a Bluetooth\* device on the platform.

### 8.2 General Purpose Signal Descriptions

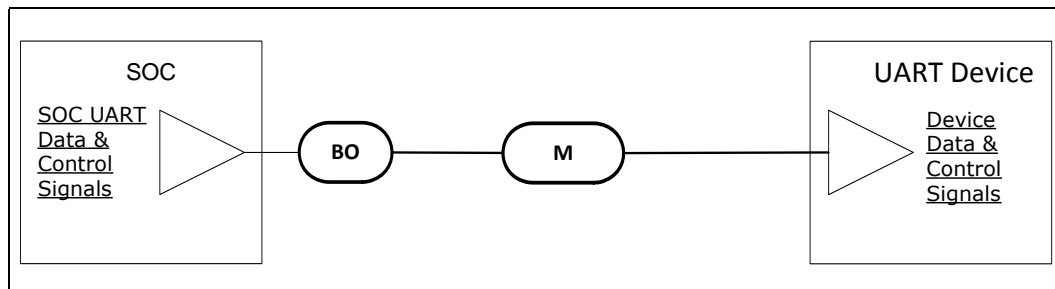
#### 8.2.1 Signal Groups

Table 31. UART Signals

Group	Signal Name	Description
Data	SIU0_RXD SIU1_RXD	Receive Data Input signals
	SIU0_TXD SIU1_TXD	Transmit Data Output signals
Control	SIU0_RTS SIU1_RTS	Request to Send signals
	SIU0_CTS SIU1_CTS	Clear to Send signals
	SIU0_DCD_B	Data Carrier Ready
	SIU0_DSR_B	Data Set Ready
	SIU0_DTR_B	Data Terminal REady
	SIU0_RI_B	Ring Indicator

### 8.3 UART Topology Guidelines

This section contains preliminary information and details for layout and routing guidelines for the UART interfaces.

**Figure 32. UART Topology**

**Table 32. UART Routing Guideline**

Parameter	Stackup (MS/SL/DSL)	Units	Routing Recommendation
M - Trace Length	MS	inch	1 - 7
M - Trace Width	MS	mils	4
M - Trace Spacing	MS	mils	5
BO - Breakout Width	MS	mils	3
BO - Breakout Spacing	MS	mils	3.5
BO - Max Breakout Length	MS	mils	500
Impedance	MS	ohm	50Ω ±15%

## 8.4 Additional Guidelines

The UART interfaces support 3.3V only. Therefore, if devices connected to the UART interfaces utilize 1.8V, external voltage translation must be implemented on the motherboard to support this configuration.

## 8.5 Terminating Unused UART Signals

If the UART functionality is not utilized, the signals should be terminated properly with external pull-up or pull-down resistors. The SOC implements internal pullup and pull down on the UART IO, see [Table 33](#).

**Table 33. UART Internal Pull Up/Down**

Pin	Direction	Pull Up/Down
SIU0_RXD SIU1_RXD	Input	Internal 20K Pull Up
SIU0_TXD SIU1_TXD	Output	No Internal Pull up or Pull Down
SIU0_RTS SIU1_RTS	Output	No Internal Pull up or Pull Down
SIU0_CTS SIU1_CTS	Input	Internal 20K Pull Up
SIU0_DCD_B	Input	Internal 20K Pull Up

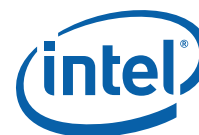


**Table 33. UART Internal Pull Up/Down**

Pin	Direction	Pull Up/Down
SIU0_DSR_B	Input	Internal 20K Pull Up
SIU0_DTR_B	Output	No Internal Pull up or Pull Down
SIU0_RI_B	Input	Internal 20K Pull Up

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## 9.0 General Purpose SPI Interface Design Guidelines

### 9.1 General Introduction

#### 9.1.1 Description

The two general-purpose SPI interfaces support various devices which use serial protocols for transferring data such as sensors on the platform.

Each interface consists of 5 wires: a clock (CLK), two chip select's (CS0 & CS1) and 2 data lines (MOSI and MISO). The CS signals are generated from GPIO pins.

The general-purpose SPI is full-duplex synchronous serial interface. The SPI interface operates in master mode only, and supports serial bit rate up to 50Mb/s. Serial data formats may range from 4 to 32 bits in length.

### 9.2 General Purpose Signal Descriptions

#### 9.2.1 Signal Groups

Table 34. SPI Signals

Group	Signal Name	Description
Clock	SPI0_SCK SPI1_SCK	Clock signals
Data	SPI0_MISO SPI1_MISO	Master In Slave Out signals
	SPI0_MOSI SPI1_MOSI	Master Out Slave In signals
Chip Select <sup>1</sup> SPI 0	GPIO[0] GPIO[1]	Chip select signals for SPI 0
Chip Select <sup>2</sup> SPI 1	GPIO[2] GPIO[3]	Chip select signals for SPI 1

1. Though SPI0\_SS\_B is available as pins in order to support multiple SPI slaves they are not utilized.
2. Though SPI1\_SS\_B is available as pins in order to support multiple SPI slaves they are not utilized.

### 9.3 Topology Guidelines

This section contains preliminary information and details for layout and routing guidelines for the general-purpose SPI interfaces.

Figure 33. SPI0 Topology

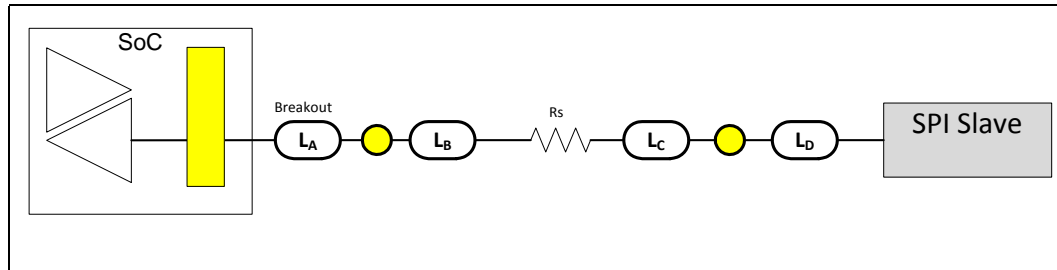


Table 35. SPI0\_MOSI, SPI0\_SCK

	Breakout			
PCB Routing Layer(s) Optional	4 Layer	4 Layer	4 Layer	4 Layer
Transmission Line Segment	$L_A$	$L_B$	$L_C$	$L_D$
Routing Layer (Microstrip / Stripline / Dual Stripline)	MS	MS	MS	MS
Characteristic Impedance (Single-ended)	50 $\Omega$ +/- 10%			
Trace Width (w)	4.2 mil	4.2 mil	4.2 mil	4.2 mil
Trace Spacing(S2): Between GPIO Signals	4.2 mil	10 mil	10 mil	4.2 mil
Trace Spacing(S3): Between GPIO and other signals	4.2 mil	10 mil	10 mil	4.2 mil
Trace Segment Length	0.5" max	0.1" - 0.8"	0.1" - 3.0"	0.5" max

**Note:** \* Keep  $L_A + L_B$  as short as possible to give the best margin on the overshoot/undershoot violation.

Table 36. SPI0\_MISO

	Breakout			
PCB Routing Layer(s) Optional	4 Layer	4 Layer	4 Layer	4 Layer
Transmission Line Segment	$L_A$	$L_B$	$L_C$	$L_D$
Routing Layer (Microstrip / Stripline / Dual Stripline)	MS	MS	MS	MS
Characteristic Impedance (Single-ended)	50 $\Omega$ +/- 10%			
Trace Width (w)	4.2 mil	4.2 mil	4.2 mil	4.2 mil
Trace Spacing(S2): Between GPIO Signals	4.2 mil	10 mil	10 mil	4.2 mil



**Table 36. SPI0\_MISO**

	Breakout			
Trace Spacing(S3): Between GPIO and other signals	4.2 mil	10 mil	10 mil	4.2 mil
Trace Segment Length	0.5" max	0.1" - 3.0"	0.1" - 0.8"	0.5" max

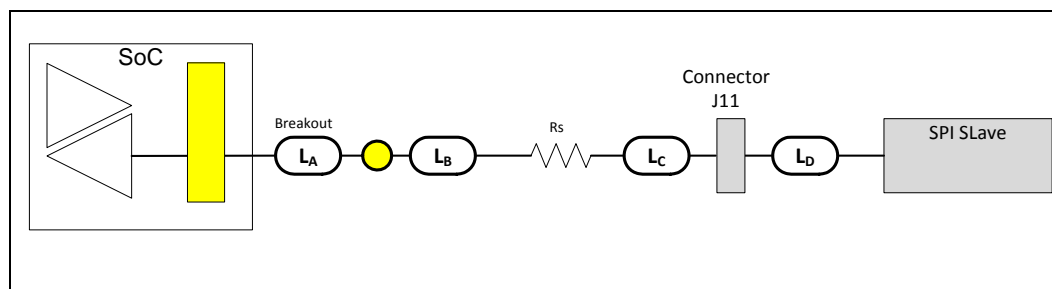
**Note:** \* Keep Lc + Ld as short as possible to give the best margin on the overshoot/undershoot violation.

Data to Clock MB length matching rule <sup>1</sup>	< 200mils
Number of vias	max 2
Rs	33ohm +/- 5%
Reference Plane	Solid Ground Reference
Buffer	c69p0cfiohvtewtop_3.3V_po lo

1. This requirement relates to the platform routing and does not include the inter package routing.

**Note:** The guidelines regarding the routing of the GPIO based CS are TBD.

**Figure 34. SPI1Topology**



**Table 37. SPI1\_MOSI, SPI1\_SCK**

	Breakout			
PCB Routing Layer(s) Optional	4 Layer	4 Layer	4 Layer	4 Layer
Transmission Line Segment	LA	LB	LC	LD
Routing Layer (Microstrip / Stripline / Dual Stripline)	MS	MS	MS	MS
Characteristic Impedance (Single-ended)	50 Ω +/- 15%			
Trace Width (w)	4.2 mil	4.2 mil	4.2 mil	4.2 mil
Trace Spacing(S2): Between GPIO Signals	4.2 mil	10 mil	10 mil	10 mil
Trace Spacing(S3): Between GPIO and other signals	4.2 mil	15 mil	15 mil	15 mil
Trace Segment Length	0.5"	min = 0.2" max = 0.8"	min = 0.1" max = 1.5"	0.25" max



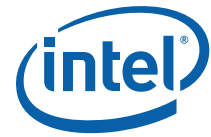
Table 38. SPI1\_MISO

	Breakout			
PCB Routing Layer(s) Optional	4 Layer	4 Layer	4 Layer	4 Layer
Transmission Line Segment	L <sub>A</sub>	L <sub>B</sub>	L <sub>C</sub>	L <sub>D</sub>
Routing Layer (Microstrip / Stripline / Dual Stripline)	MS	MS	MS	MS
Characteristic Impedance (Single-ended)	50 Ω +/- 15%			
Trace Width (w)	4.2 mil	4.2 mil	4.2 mil	4.2 mil
Trace Spacing(S2): Between GPIO Signals	4.2 mil	10 mil	10 mil	10 mil
Trace Spacing(S3): Between GPIO and other signals	4.2 mil	15 mil	15 mil	15 mil
Trace Segment Length	0.5"	min = 0.1" max = 1.5"	min = 0.2" max = 0.8"	0.25" max

Data to Clock MB length matching rule <sup>1</sup>	< 200mils
Number of vias	max 1
Rs	33ohm +/- 5%
Reference Plane	Solid Ground Reference

1. This requirement relates to the platform routing and does not include the inter package routing.

Note: The guidelines regarding the routing of the GPIO based CS are TBD.



## 9.4 Terminating Unused SPI Signals

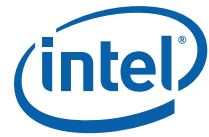
If the SPI functionality is not utilized, the signals should be terminated properly with external pull-up or pull-down resistors.

**Table 39. SOC SPI Internal Pull Up/ Pull Down**

Pin	Direction	Status
SPI0_MISO	Input	Internal 20K Pull up
SPI1_MISO	Input	Internal 20K Pull up
SPI0_MOSI	Output	External Weak Pull Up or Pull Down
SPI1_MOSI	Output	External Weak Pull Up or Pull Down
SPI0_SCK	Output	External Weak Pull Up or Pull Down
SPI1_SCK	Output	External Weak Pull Up or Pull Down

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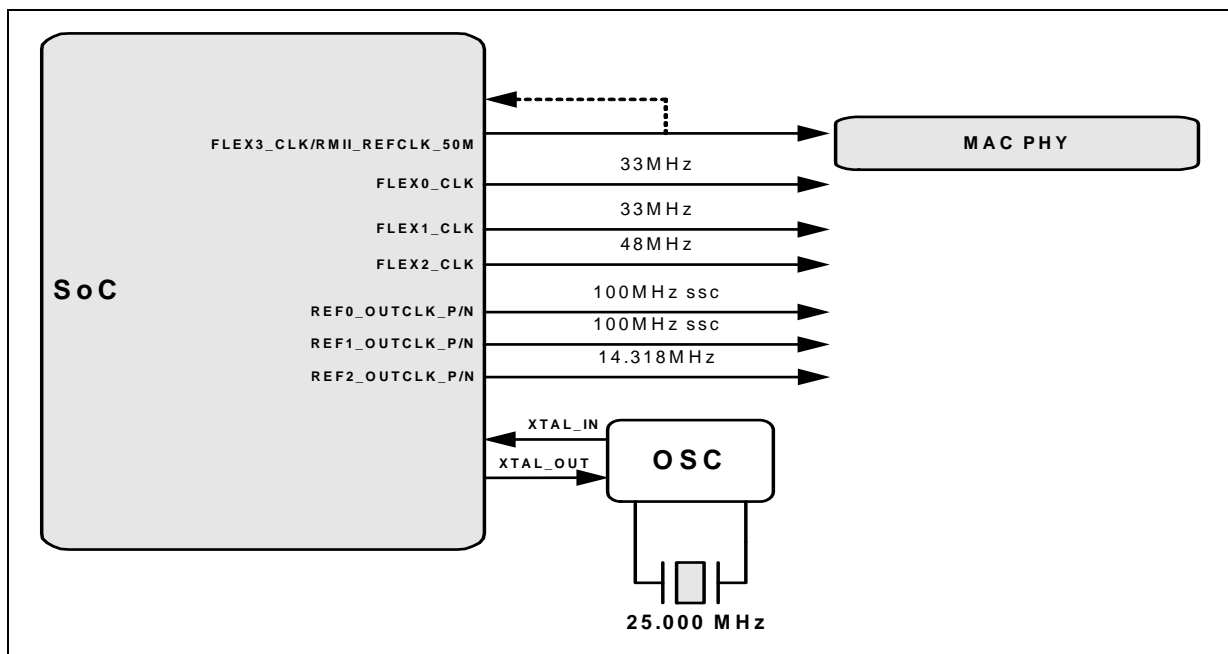
## 10.0 Platform Clocks Design Guidelines

### 10.1 Platform Clock General Introduction

#### 10.1.1 Description

Intel® Quark SoC X1000 implements full integrated clocking mode as the default platform clock solution. In the full-clock integration mode, a 25 MHz crystal oscillator provides the input clock to the Intel® Quark SoC X1000 integrated clock controller and SoC generates the output clocks that are required by all the platform components.

Figure 35. Clock Integration Distribution Diagram



Note: REF0\_OUTCLK and REF0\_OUTCLK default to SSC mode (Spread Spectrum Clock)



A 25 MHz crystal will be connected to the SoC as an input. This crystal input is used to generate the following platform clock outputs:

- 1x 50 MHz differential sources for RMII\_REFCLK\_50M
- Two 33 MHz single ended clocks.
- 48 MHz single ended clock.
- Two 100 MHz differential clocks which default to spread spectrum mode.
- One 14.318 MHz differential clock.

*Note:* **25 MHz Crystal Requirement:** All SoC-based platforms must use a 25 MHz crystal on the platform to generate a differential clock on XTAL\_IN/OUT to enable SoC to generate platform clocks. It is critical that this XTAL clock is of good quality and has minimal interference to ensure correct locking of the internal PLL. Intel is not validating use of an external clock buffer oscillator connection to XTAL pins.

*Note:* **Unused SoC Clock Outputs:** All unused clocks on SoC can be left as No Connect.

## 10.2 Platform Reference Clock Signal Descriptions

Table 40. Signal Groups

Clock Type	Clock Signals	Description
Input from 25 MHz crystal (Required)	XTAL_IN/XTAL_OUT	25 MHz source clock for Full Clock Integrated mode
Output Clocks from SoC	CLKSYS25_OUT	Single-ended 25 MHz output to devices.
	REF0_OUTCLK_P REF0_OUTCLK_N REF1_OUTCLK_P REF1_OUTCLK_N REF2_OUTCLK_P REF2_OUTCLK_N	REF0_CLK: 100MHz 1v differential REF1_CLK: 100MHz 1v differential REF2_CLK: 14.318MHz 1v differential
	SPI_CLK	SPI Clocks from SoC
	FLEX0_CLK FLEX1_CLK FLEX2_CLK RMII_REF_CLK_OUT	FLEX0_CLK 33.33MHz 3.3v FLEX1_CLK 33.33MHz 3.3v spread spectrum FLEX2_CLK 48MHz 3.3v Reference clock for RMII interface



## 10.3 Platform Clocks Topology Guidelines

### 10.3.1 Differential Clock Routing Topology

The following SoC clock outputs utilize the guidelines in this section:

- Differential reference clocks, e.g., REF0\_CLK\_P/N

Figure 36. Differential Clock Topology for SoC to Clock Receiver

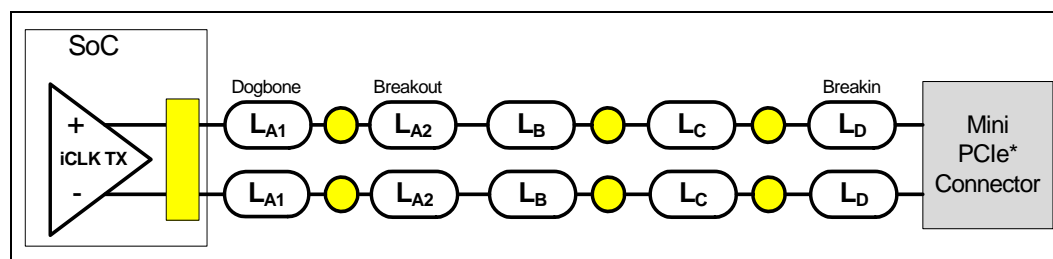


Table 41. Differential Clock Routing Guidelines

REFCLK0_P & REFCLK0_N	Dogbone	Breakout	Main Route 1		Breakin
PCB Routing Layer(s) Optional	4 Layer	4 Layer	4 Layer	4 Layer	4 Layer
Transmission Line Segment	L <sub>A1</sub>	L <sub>A2</sub>	L <sub>B</sub>	L <sub>C</sub>	L <sub>D</sub>
Routing Layer (Microstrip / Stripline / Dual Stripline)	MS	MS	MS	MS	MS
Characteristic Impedance (Differential)	100 Ω +/- 10%				
Trace Width (w)	4.0 mil	4.0 mil	4.0 mil	4.0 mil	4.0 mil
Trace Spacing (S1): Between P and N of clock pair	4.0 mil	4.0 mil	15 mil	15 mil	15 mil
Trace Spacing (S2): Between different Clock pairs	6.0 mil	6.0 mil	20 mil	20 mil	20 mil
Trace Spacing (S3): Between Clock pairs and other signals	6.0 mil	6.0 mil	20 mil	20 mil	20 mil
Trace Segment Length	0.05" max	0.5" max	1.5" max	0.2" max	0.5" max
<b>Note:</b> Can support up to 2" on the Mini PCIe Card					

Length Matching between P and N within a diff. pair	Match segments <=10 mils Match overall length <=10 mils
Number of vias	max 3
Reference Plane	Continuous Ground only

### 10.3.1.1 Differential Routing Considerations

When routing differential clocks, note the following recommendations:

- Ground referencing is preferred. However, differential clocks can be routed referenced to other planes through the use of stitching capacitors to provide the appropriate decoupling where the signal crosses planes.
- Do not split up the two halves of a differential clock pair between layers. Route to all agents on the same physical routing layer referenced to ground.
  - Typical routing assumes 1 layer transition within 500 mils of the SoC package and a second layer transition within 500 mils of the destination ball.
  - If a layer transition is required, both clock traces of the differential clock pair must transition layers at the same length  $\pm 100$  mils.
  - If an additional layer transition is required, use simulations to ensure the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Do not place vias between adjacent complementary clock traces and avoid differential vias. Vias, placed in one signal of a differential-pair must be matched by a via in the complement. Differential vias can be placed within length BO if needed to shorten length BO.

No length matching is required between different source pairs.

### 10.3.1.2 Stitching Via Usage and Placement

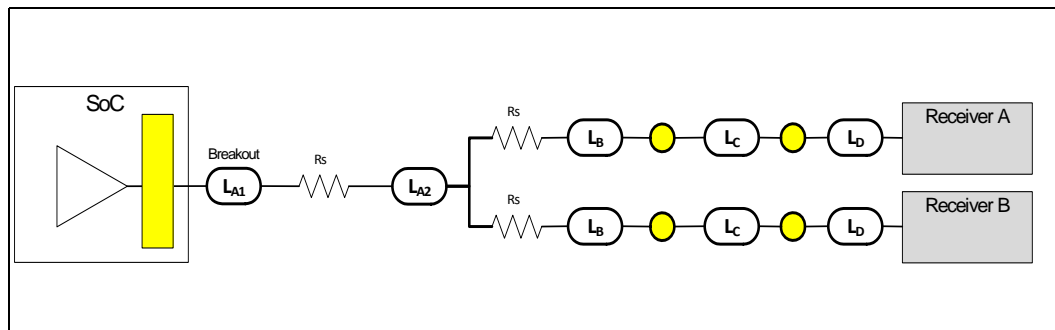
Stitching vias must be used when signal traces change layers from top layer to bottom or internal layer. In these cases reference GND layer associated with top signal layer has to be connected with GND reference layer associated with bottom or internal signal layer using GND stitching via. Placing GND stitching via according current guidelines maintains optimal current return path and minimize crosstalk effect.

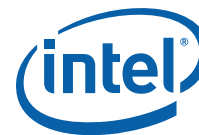
- Stitching vias should be placed with this spacing:
  - 30-mils (0.762-mm) pitch between differential clock via and closest stitching GND-via.
  - Every differential clock via must have at least one GND stitching via with a maximum spacing of 30 mils (0.762 mm).
- Placement of additional stitching vias, where possible, is recommended.

Motherboard GND stitching vias placement for differential clock signals.

## 10.3.2 Single Ended Clock Routing Topology

Figure 37. Single Ended Clock Topology for SoC



**Table 42. iClock (Single-ended Clocks)**

For the Intel® Quark SoC X1000 use case, one of the flex clocks, Flex3 clock, is used as a reference to the RMI. This clock is routed to the PHY and also back the SoC integrated MAC.

<b>FLEX3_CLK 50 MHz</b>	<b>Breakout</b>				
<b>PCB Routing Layer(s) optional</b>	4 Layer	4 Layer	4 Layer	4 Layer	4 Layer
<b>Transmission Line Segment</b>	L <sub>A1</sub>	L <sub>A2</sub>	L <sub>B</sub>	L <sub>C</sub>	L <sub>D</sub>
<b>Routing Layer (Microstrip / Stripline / Dual Stripline)</b>	MS	MS	MS	MS	MS
<b>Characteristic Impedance (Single-ended)</b>	50 Ω +/- 15%				
<b>Trace Width (w)</b>	4.2 mil	4.2 mil	4.2 mil	4.2 mil	4.2 mil
<b>Trace Spacing(S2): Between Single-ended Clocks</b>	4.2 mil	20 mil	20 mil	20 mil	20 mil
<b>Trace Spacing(S3): Between Clock and other signals</b>	4.2 mil	20 mil	20 mil	20 mil	20 mil
<b>Trace Segment Length</b>	0.5" max	0.8" max	0.2" max	6" max	1" max
	L <sub>A</sub> + L <sub>A2</sub> ≤ 500 mil				

<b>Length Matching between Single-ended Clocks</b>	Total trace length from SoC output (RMII_REF_CLK_OUT) to external PHY must match the trace length from SoC Output (RMII_REF_CLK_OUT) to SoC input (RMII_REF_CLK) within 10mils.
<b>Rs</b>	22 ohm +/- 5%
<b>Number of vias</b>	max 2
<b>Reference Plane</b>	Continuous Ground only
<b>Note</b>	Only legacy signal allows to route close with 3x spacing (total length <3")

The single ended clocks are driven via clock drivers. The package and board routes should be treated similarly to differential clock routes. They should be fully shielded on both sides with VSS and the VCC that is applicable to the driver, and with spacing equal to or greater than the standard clock routes should be maintained. They should not be routed over the XTAL\_IN and XTAL\_OUT traces.

## 10.4 25 MHz Crystal and Associated RC Components

Platforms are required to use the 25 MHz crystal to generate all platform clocks. This requires that on board the following components should be stuffed:

- A 25 MHz crystal
- 2 External Load Capacitors Ce1 and Ce2
- A 1-MΩ bias resistor

Refer to [Figure 38](#) below for illustration of the 25 MHz crystal connectivity.



### 10.4.1 Crystal External Load Capacitor Requirements

The 25 MHz crystal is physically tuned to operate within the specified frequency range and ppm tolerance with a certain expected capacitive load present. The expected external capacitive load to be used ( $C_e$ ) consists of the crystal capacitive load plus the pin and trace capacitances. The external load capacitors are important to minimize frequency variations from the crystal by compensating for variable PCB factors related to pin and trace capacitance. Care must be exercised in the selection of the external load capacitors to present the expected capacitive load specified for the crystal in use on the platform.

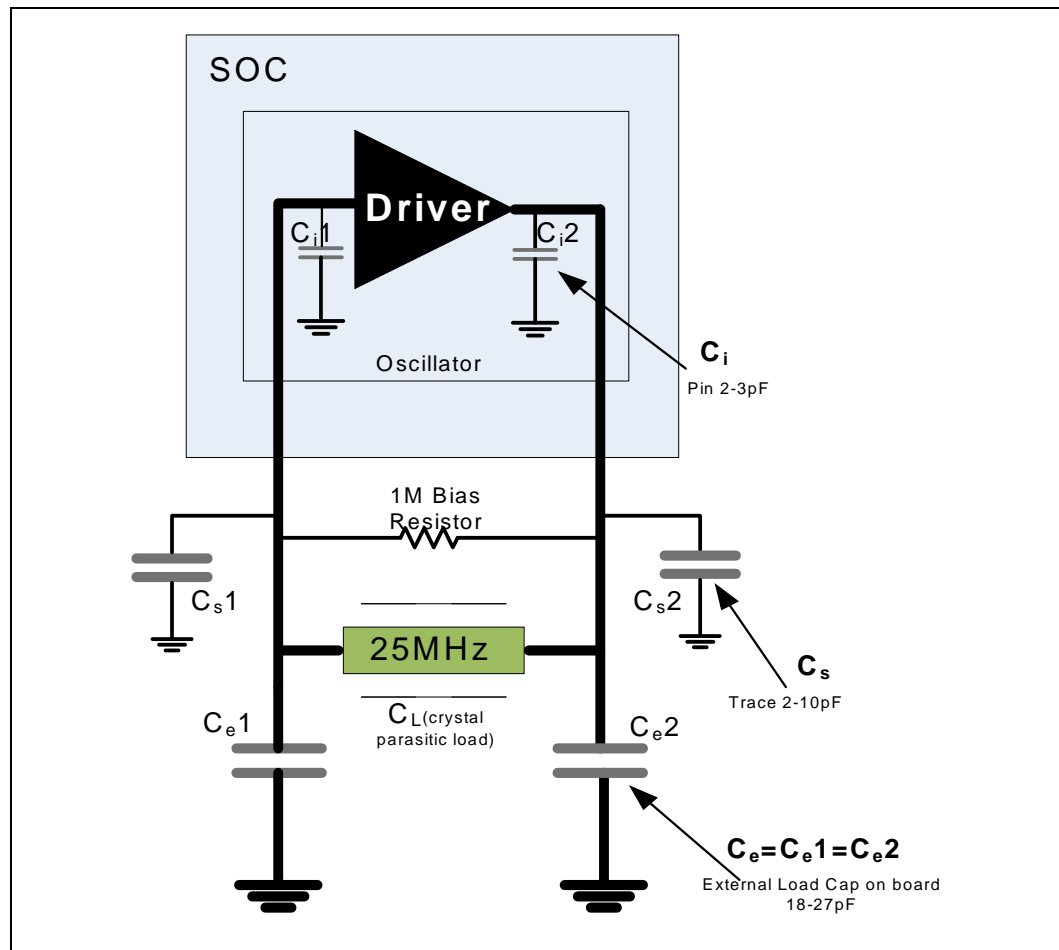
The appropriate capacitor value for the platform may be determined using the following formula:

$C_e = 2 * C_L - (C_s + C_i)$ , where:

- $C_e$  = External Load Capacitor Value; (18-27 pF)
- $C_L$  = Specified Crystal Capacitive Load; (Can be found from crystal datasheet)
- $C_s$  = Board Trace Capacitance (includes crystal pad capacitance); (2-10 pF)
- $C_i$  = SoC Pin Capacitance; (2-3 pF)

Figure 38 illustrates the crystal external load capacitor parameters. Due to vendor variation in crystal characteristics, layout variations and PCB trace capacitance differences, the above calculation should be performed for each design to determine the precise value of  $C_e$  that is optimal for the particular platform.

Figure 38. 25 MHz Crystal External Load Capacitor Parameters



#### 10.4.2 25 MHz Crystal Routing Considerations

- Short (< than 1250 mils) shielded traces on XTAL\_IN/XTAL\_OUT to minimize cross-talk induced jitter.
- Shield XTAL\_IN/XTAL\_OUT signals and reference to ground planes.
- Highly recommended to not route high frequency signals directly below the crystal.

*Note:* The oscillator signals are very sensitive to board noise due to very slow shape of waveforms (sine waves). Care should be taken to provide shielding from any noisy signals near traces or under the components associated with oscillator.

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## 11.0 SPI Flash Design Guidelines

### 11.1 Serial Peripheral Interface (SPI) General Introduction

The following provides general guidelines for compatibility and design recommendations for supporting flash devices.

#### 11.1.1 Description

Intel® Quark SoC X1000 supports three integrated Serial Peripheral Interface (SPI) 4-pin interfaces that provides a potentially lower-cost alternative for system flash. The Legacy SPI interface is specifically for the system boot flash and the additional two interfaces are for general purpose use. Each Serial Peripheral Interface is used to support a SPI compatible flash device via an independent GPIO chip select pin. Each SPI flash device can be up to 64 MBytes (512 Mbits). SoC drives the SPI Interface at either 20 MHz (legacy SPI) or 25MHz.

### 11.2 Serial Peripheral Interface (SPI) Signal Description

Table 43. SPI Signals

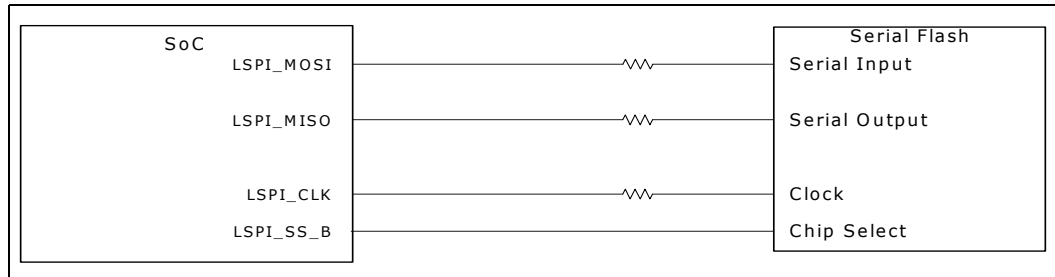
Signal Name	Group	Description
LSPI_MOSI	Data	Legacy SPI serial output data from Intel® Quark SoC X1000 to the SPI flash device.
LSPI_MISO	Data	Legacy SPI serial input data from the SPI flash device to Intel® Quark SoC X1000.
LSPI_CLK	Clock	Legacy SPI Clock output from Intel® Quark SoC X1000
LSPI_SS_B	Chip Select	Legacy SPI chip select
SPI0_MOSI SPI1_MOSI	Data	SPI serial output data from Intel® Quark SoC X1000 to the SPI flash device.
SPI0_MISO SPI1_MISO	Data	SPI serial input data from the SPI flash device to Intel® Quark SoC X1000
GPIO[0] GPIO[1]	Chip Select	SPI chip selects for SPI 0 Interface
GPIO[2] GPIO[3]	Chip Select	SPI chip select for SPI 1 Interface
SPI0_SCK SPI1_SCK	Clock	SPI Clock output from

### 11.3 Serial Peripheral Interface (SPI) Topology Guidelines

This section contains preliminary information and details for layout and routing guidelines for Intel® Quark SoC X1000 SPI interface. The Legacy SPI flash must be directly connected to the Intel® Quark SoC X1000 Legacy SPI bus in all SKUs. Also, refer to the Serial Flash vendor documentation for additional Serial Flash specific design considerations.

#### 11.3.1 SPI Single Flash Device Topology Guidelines

Figure 39. Legacy SPI Topology (Single Device)



##### 11.3.1.1 SPI Single Flash Device Routing Guideline

Figure 40. SPI Single Flash Device Routing Guidelines for LSPIO\_MOSI, LSPIO\_MISO, LSPIO\_CS\_N, LSPIO\_SCK

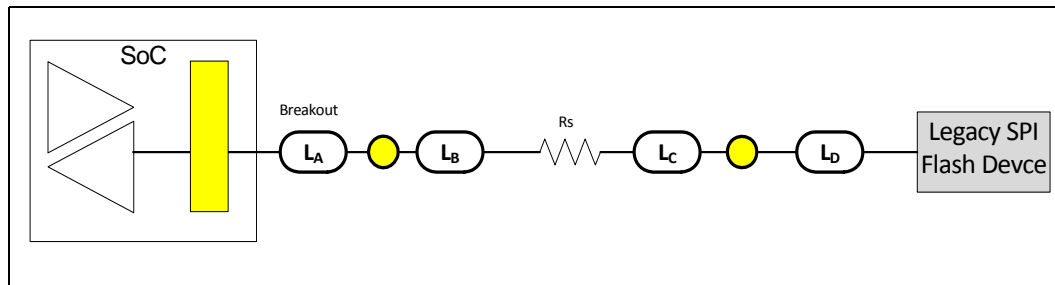


Table 44. LSPIO\_MOSI, LSPIO\_MISO, LSPIO\_CS\_N, LSPIO\_SCK (Sheet 1 of 2)

	Breakout			
PCB Routing Layer(s) Optional	4 Layer	4 Layer	4 Layer	4 Layer
Transmission Line Segment	L <sub>A</sub>	L <sub>B</sub>	L <sub>C</sub>	L <sub>D</sub>
Routing Layer (Microstrip / Stripline / Dual Stripline)	MS	MS	MS	MS
Characteristic Impedance (Single-ended)	50 Ω +/- 10%			
Trace Width (w)	4.2 mil	4.2 mil	4.2 mil	4.2 mil
Trace Spacing(S2): Between GPIO Signals	4.2 mil	10 mil	10 mil	4.2 mil



**Table 44. LSPIO\_MOSI, LSPIO\_MISO, LSPIO\_CS\_N, LSPIO\_SCK (Sheet 2 of 2)**

<b>Trace Spacing(S3): Between GPIO and other signals</b>	4.2 mil	10 mil	10 mil	4.2 mil
<b>Trace Segment Length</b>	0.5" max	0.1" - 0.8"	0.1" - 3.0"	0.5" max

**Note:** \* Keep La + Lb as short as possible to give the best margin on the overshoot/undershoot violation.

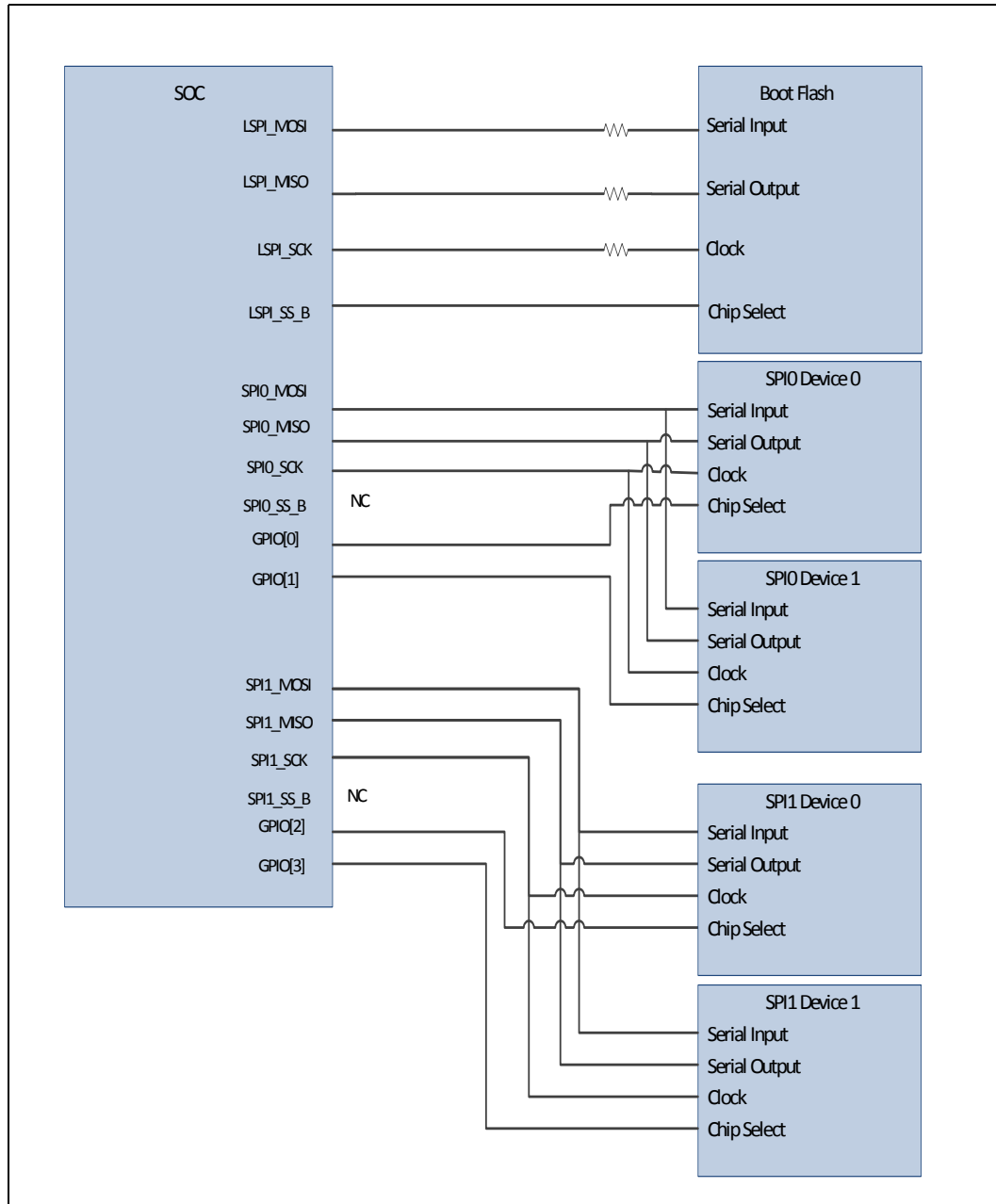
**11.3.1.2 SPI Single Flash Device Length Matching Requirement**

- LSPI\_SCK & LSPI\_MOSI must be length matched to within 500mils.
- LSPI\_SCK & LSPI\_SS\_B must be length matched to within 500mils.

### 11.3.2 Dual SPI Devices + Bootflash Topology Guidelines

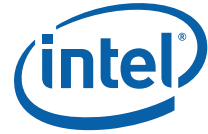
Topology below is a full configuration which consists of 4 SPI Slaves and 1 Bootflash device. System can be configured with less SPI Slaves but always 1 Bootflash device.

Figure 41. SPI Topology (4 SPI Devices + Legacy SPI Device)



#### 11.3.2.1 Multiple SPI Flash Device + Bootflash Routing Guideline

*Note:* SPI\_CLK must be 20mils spacing from any other high frequency (>1GHz) signal.



### 11.3.2.2 Dual SPI Flash Device Routing Guideline

- SPI\_CLK & SPI\_MOSI (including all the Master Output Pins during Dual Operation) must be length matched to within 500mils.
- SPI\_CLK & GPIO[x] must be length matched to within 500mils.
- SPI branches (segment M2) need to have length matching of +/- 100mils.

### 11.3.3 Boot BIOS Destination

Intel® Quark SoC X1000 can only boot via the Legacy SPI interface, SPI0 and SPI1 can be used for non-volatile data.

## 11.4 Serial Flash Vendors

The following list of vendors manufacture serial flash devices should not be considered as Intel Approved Devices or vendors. But these devices conform to Intel's specific requirements. For additional details on the compatibility requirements for SPI devices refer to the latest SoC EDS. Contact the flash vendor directly for information on packaging and density.

VENDOR	WEBSITE
ATMEL	<a href="http://www.atmel.com/">http://www.atmel.com/</a>
MACRONIX	<a href="http://www.mxix.com.tw">http://www.mxix.com.tw</a>
SST/MICROCHIP	<a href="http://www.microchip.com">http://www.microchip.com</a>
NUMONYX/MICRON	<a href="http://www.micron.com/">http://www.micron.com/</a>
WINBOND	<a href="http://www.winbond.com/">http://www.winbond.com/</a>
SPANSION	<a href="http://www.spansion.com/">http://www.spansion.com/</a>
EON	<a href="http://www.eonssi.com/">http://www.eonssi.com/</a>
AMIC	<a href="http://www.amictechnology.com">http://www.amictechnology.com</a>
GIGADEVICE	<a href="http://www.gigadevice.com">http://www.gigadevice.com</a>
FIDELIX	<a href="http://www.fidelix.co.kr/">http://www.fidelix.co.kr/</a>
Chingis Technology	<a href="http://www.chingistek.com/">http://www.chingistek.com/</a>
PMC	<a href="http://www.pmcflash.com/">http://www.pmcflash.com/</a>

**Note:** OEMs must fully validate any SPI flash device to ensure compatibility with their platforms. This should not be considered a complete list of SPI vendors and is not an indication of Intel approved devices or vendors. Please contact your preferred flash vendor directly to determine if they have a compatible device.







## 12.0 RTC Design Guidelines

### 12.1 Real Time Clock General Introduction

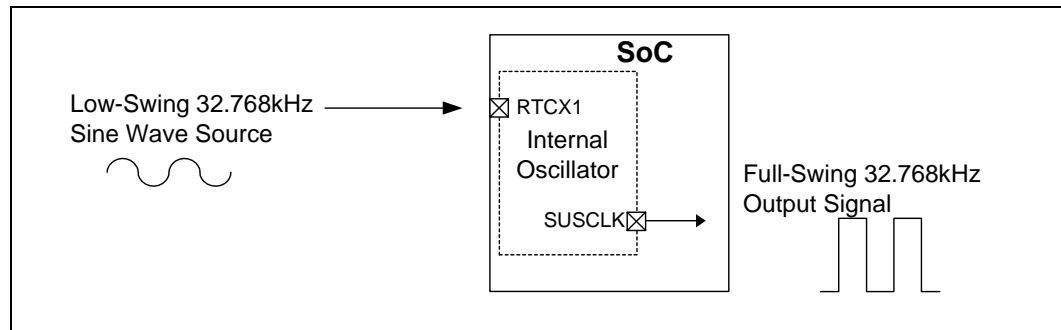
#### 12.1.1 Description

The Intel® Quark SoC X1000 contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

SoC RTC module defaults to using an internal clock source alternatively an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 43 shows the external circuitry that comprises the oscillator of SoC RTC.

The SoC uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the SoC, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output from the RTC for internal system use. This is illustrated in Figure 42.

Figure 42. RTCX1 and RTCX2 Relationship in SoC



### 12.2 Real Time Clock Signal Descriptions

#### 12.2.1 Signal Groups

Table 45. RTC Signals

Section	Group	Signals	Description
Section 12.3.2	Crystal Input 1	RTCX1	Crystal Input 1
Section 12.3.2	Crystal Input 2	RTCX2	Crystal Input 2
Section 12.5	Reset	RTCST# (I_1PAD)	RTC Reset



Table 45. RTC Signals

Section	Group	Signals	Description
Section 12.2.2	Status	S5_PG (I_2PAD)	Platform S5 Power Good.
	Status	RTC_EXT_CLKEN_B (I_4_PAD)	External RTC Clock source enable
	Status	S0_PG (I_5PAD)	Platform S0 Power Good

### 12.2.2 State Power Good Indicators

S5\_PG is an indicator from the platform that the S5 input rails are at 90% of their nominal value. The use of a voltage regulator spec'ed to output a power good at the required level is optimal but a discrete circuit is also applicable.

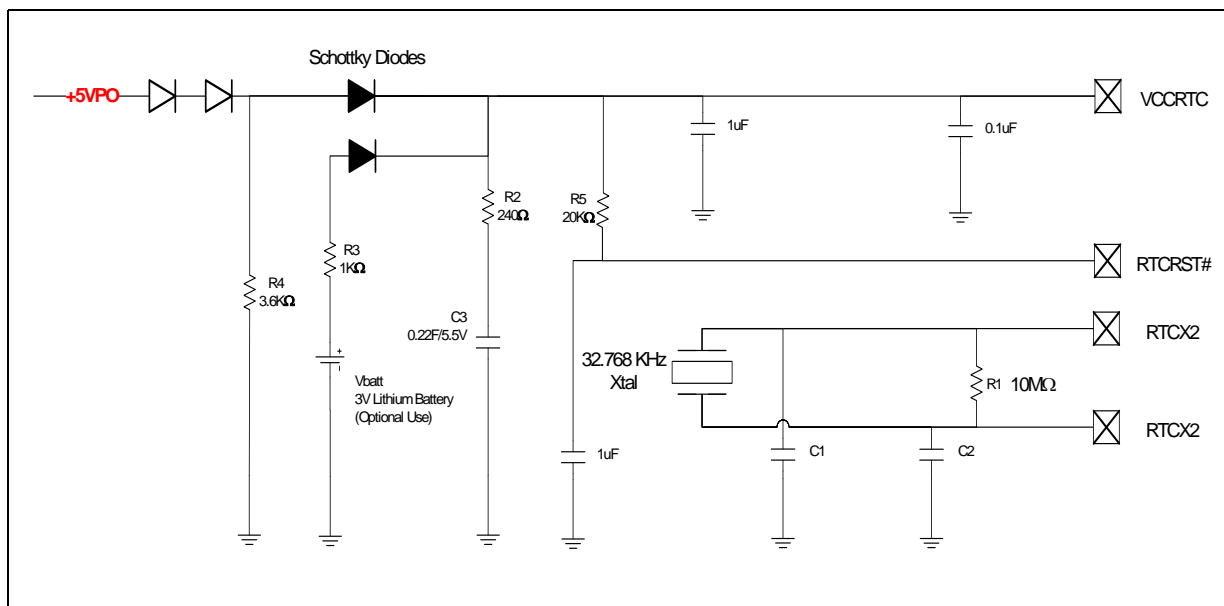
S0\_PG is an indicator from the platform that the S0 input rails are at 90% of their nominal value. The use of a voltage regulator spec'ed to output a power good at the required level is optimal but a discrete circuit is also applicable.



## 12.3 Real Time Clock Topology Guidelines

### 12.3.1 RTC External Example Circuit

Figure 43. Example External Circuitry for the SoC RTC



**Notes:**

1. Reference designators are arbitrarily assigned.
2. +5vPO is active whenever the system is plugged in.
3. Vbatt is voltage provided by the battery and is optional.
4. VccRTC, RTCX1, and RTCX2 are Intel SoC pins.
5. VccRTC powers SoC RTC well.
6. RTCX1 is the input to the internal oscillator. RTCX1 can be driven by external clock generator to desired frequency.
7. RTCX2 is the feedback for the external crystal. When single ended external clock generator is used, this pin should be grounded.
8. R1 = 10MΩ, R2 = 240Ω, R3 = 1KΩ, R4 = 3.6KΩ, R5 = 20KΩ.
9. The exact capacitor values for C1 and C2 must be based on the crystal maker recommendations. Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.
10. C3 = 0.22F/5.5V. Panasonic SD Series Super Cap,EEC-SDHD224V, ESR=75Ω.
11. Schottky Diodes (Black) are MBR0504T1G, Regular diodes are 1N4148, IN914 equivalents.

Table 46. RTC Routing Guidelines

Parameter	Segment/Signal Name	Stackup (MS/SL/DSL)	Units	Routing Recommendation
Total Length	RTCX1 RTCX2	MS	mils	1,000
Resistor	R1	NA	MΩ	10

**Notes:**

1. Spacing, S > 15 mils (0.381 mm).



### 12.3.2 General RTC Layout Considerations

The Intel® Quark SoC X1000 operates in an internally source RTC clock mode by default, the external RTC clock is required in cases where the SoC will be shutdown to G3. In G3 the RTC is powered via battery backup and the RTC clock is sourced from an 32kHz platform crystal. The use of an external RTC clock source allows the use of a more precise 32kHz clock.

Since the RTC circuit is very sensitive and requires highly accurate oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. Intel SoC recommends a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn ball). Keep routing on the RTC circuit basic to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR4, a 5-mil trace has approximately 3.3 pF per inch.
- Reduce trace signal coupling by avoiding routing of adjacent PCI signals close to RTCX1 and RTCX2.
- Using a ground guard plane is highly recommended.

The oscillator VCC should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

### 12.3.3 External Capacitors

To maintain the RTC accuracy, the external capacitor values  $C_1$  and  $C_2$  should be chosen to provide the manufacturer's specified load capacitance ( $C_{load}$ ) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{load} = \frac{[(C_1 + C_{in1} + C_{trace1}) \cdot (C_2 + C_{in2} + C_{trace2})]}{[(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}}$$

Where:

$C_{load}$  = Crystal's load capacitance. This value can be obtained from Crystal's specification.

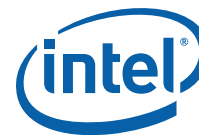
$C_{in1}$ ,  $C_{in2}$  = input capacitances at RTCX1, RTCX2 balls of SoC. These values can be obtained in the SoC data sheet.

$C_{trace1}$ ,  $C_{trace2}$  = Trace length capacitances measured from Crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. A typical value, based on a 5 mil wide trace and a ½ ounce copper pour, is approximately equal to:

$$C_{trace} = \text{trace length} \cdot 4\text{pF/inch}$$

$C_{parasitic}$  = Crystal's parasitic capacitance. This capacitance is created by the existence of 2 electrode plates and the dielectric constant of the crystal blank inside the Crystal part. Refer to the crystal's specification to obtain this value.

Ideally,  $C_1$ ,  $C_2$  can be chosen such that  $C_1 = C_2$ . Using the equation of  $C_{load}$  above, the value of  $C_1$ ,  $C_2$  can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However,  $C_2$  can be chosen such that  $C_2 > C_1$ . Then  $C_1$  can be trimmed to obtain the 32.768 kHz.



In certain conditions, both C1, C2 values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C1, C2 value are smaller than the theoretical values, the RTC oscillation frequency will be higher.

The following example illustrates the use of the practical values C1, C2 in the case that theoretical values cannot guarantee the accuracy of the RTC in low temperature condition:

**Example:**

According to a required 12 pF load capacitance of a typical crystal that is used with the SoC, the calculated value of C1 = C2 is 10 pF at room temperature (25 °C) to yield an 32.768 kHz oscillation.

At 0 °C the frequency stability of crystal gives -23 ppm (assumed that the circuit has 0 ppm at 25 °C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C1, C2 are chosen to be 6.8 pF instead of 10 pF, this will make the RTC oscillate at higher frequency at room temperature (+23 ppm), but this configuration of C1, C2 makes the circuit oscillate closer to 32.768 kHz at 0 °C. The 6.8 pF value of C1 and C2 is the **practical value**.

*Note:* The temperature dependency of crystal frequency is a parabolic relationship (ppm / degree squared). The effect of changing crystal's frequency when operating at 0 °C (25 °C below room temperature) is the same when operating at 50 °C (25 °C above room temperature). See crystal datasheet for more details.

## 12.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while SoC is not powered by the system.

Example batteries are: Duracell 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 6 µA, the battery life will be at least:

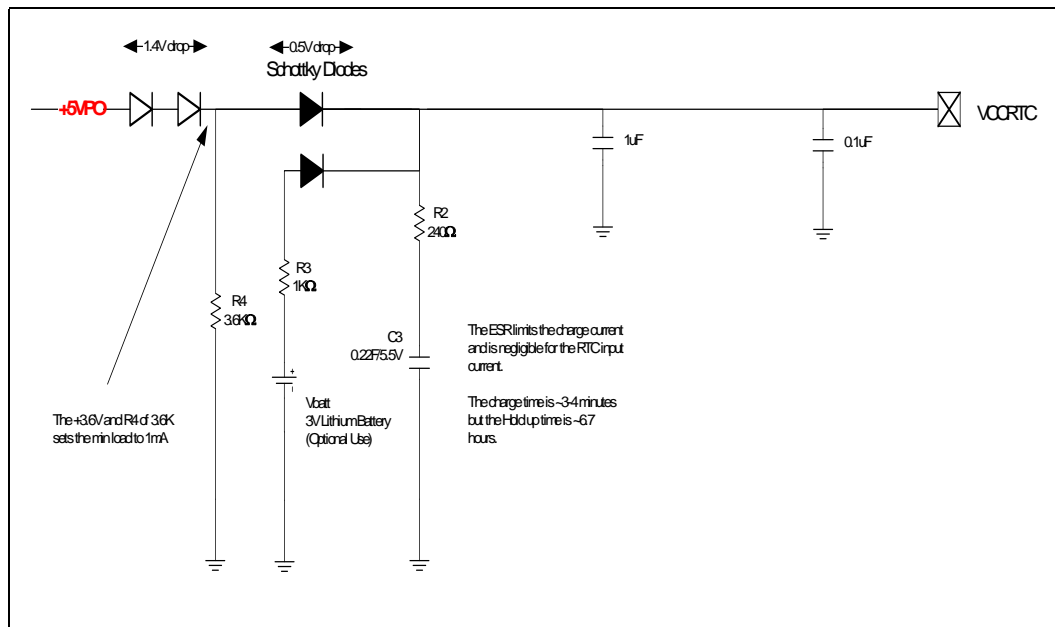
$$170,000 \mu\text{Ah} / 6\mu\text{A} = 28,333 \text{ h} = 3.2 \text{ years.}$$

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases.

The battery must be connected to SoC via an isolation Schottky diode circuit. The Schottky diode circuit allows SoC RTC well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available.

[Figure 44](#) is an example of a diode circuit that is used.

Figure 44. A Schottky Diode Circuit to Connect RTC External Battery



A standby power supply should be used in a mobile system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

Using a rechargeable coin battery or a capacitor with a short projected discharged time can increase the risk of:

- unusable anti-replay blobs

### 12.4.1 RTC Holdup Calculation

The example in Figure 44 shows Super Capacitor, C3, this is a Panasonic SD Series Super Cap, value 0.22uF/5.5V. The Panasonic EEC-SDHD224V is used in this example circuit. The SDHD224V has a ESR of 75Ω.

The discharge time is calculated as follows;

$$T = -RC \times \ln(V/V_0)$$

R: The RTC load =  $3V/12\mu A^1 = 250000$ .

C: The Super Cap = 0.22F

Therefore RC = 55000

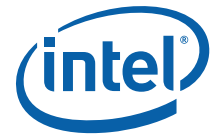
The discharge slope is based on a natural log,  $\ln(V/V_0)$  from 3.6V to 2V

V: 2V, minimum RTC operational voltage.

$$\ln(V/V_0) = \ln(2/3.6) = -0.43825$$

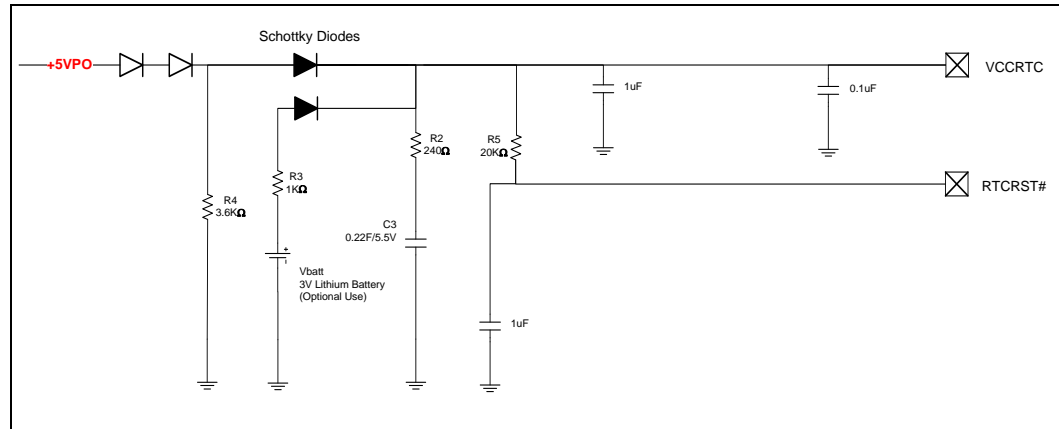
$$\text{Discharge time (T)} = -55000 \times -0.43825 = 24104 \text{ sec} = \sim 6.7 \text{ hours.}$$

1. Estimated load at 12uA



## 12.5 RTC External RTCRST# Circuit

Figure 45. RTCRST# External Circuit for the SoC RTC



SoC RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18 ms – 25 ms. When RTCRST# is asserted, bit 2 (RTC\_PWR\_STS) in the GEN\_PMCON\_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

The RTCRST# signal may also be used to detect a low battery voltage. RTCRST# will be asserted during a power up from G3 state if the battery voltage is below 2 V. This will set the RTC\_PWR\_STS bit as described above. If desired, BIOS may request that the user replace the battery.

This RTCRST# circuit is combined with the diode circuit (shown in Figure 44) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 45 is an example of this circuitry that is used in conjunction with the external diode circuit.

Table 47. RTC External RTCRST# Routing Guidelines

Parameter	Segment/Signal Name	Stackup (MS/SL/DSL)	Units	Routing Recommendation
Total Length	RTCRST#	MS	mils	8,000
Resistor	R	NA	kΩ	10
Capacitor	C	NA	uF	1

**NOTES:**

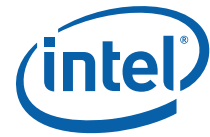
1. Impedance Target 50 Ω ±15% for Microstrip.
2. Spacing, S > 15 mils (0.381 mm).
3. RC time delay between 18 ms-25 ms must be met.
4. Spacing, S > 15 mils (0.381 mm).



## 12.6 RTC-Well Input Strap Requirements

All RTC-well inputs must be either pulled up to VccRTC or pulled down to ground while in the G3 state. RTCRST#, when configured as shown in [Figure 45](#) meets this requirement. This will prevent these nodes from floating in G3, and correspondingly will prevent I<sub>CC</sub>RTC leakage that can cause excessive coin-cell drain. The RTC\_EXT\_CLK\_EN\_B input signal should also be configured with an external weak pull-down, which selects the external RTC clock source, if operating from a battery in G3.

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## 13.0 Asynchronous Signals Design Guidelines

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### 13.1 Asynchronous Signals General Introduction

#### 13.1.1 Description

This section describes the topologies and layout recommendations for the asynchronous signals. Refer to the *Intel® Quark SoC X1000 Datasheet* for more details.

### 13.2 Asynchronous Signal Descriptions

#### 13.2.1 Signal Groups

Table 48. Asynchronous Legacy Signal Group

Signal Name	Description
GPIO[7:0]	General Purpose IO configurable in direction.

### 13.3 Asynchronous Signals Topology Guidelines

This section describes topologies and layout recommendations for the legacy signals. Although these signals toggle with relatively low frequency, most of them have very high-edge rates.

**Warning:** Inappropriate routing or lack of termination can seriously decrease signal quality and lead to electrical specification violations and even logical system failures. The following guidelines apply to all legacy signals described in this section.

- Watch for termination recommendations. If any of the signals that require platform termination are pulled-up to a voltage higher than VCCST then the reliability and power consumption of the SOC may be affected. Therefore, it is very important to follow the recommended pull-up voltage for these signals.
- The routing guidelines allow the asynchronous signals to be routed using microstrip using  $50\ \Omega \pm 15\%$  characteristic trace impedance
- Changing reference plane is not recommended and may cause signal integrity degradation. In any case, if such routing can't be avoided, use stitching vias and bypass capacitors between the reference planes near the layer transition.

General trace spacing requirements (for  $50\ \Omega$  characteristic impedance traces) specified in the following table. W is trace width and S is the space between 2 adjacent traces.

**Table 49. Asynchronous Signal General Routing Guideline**

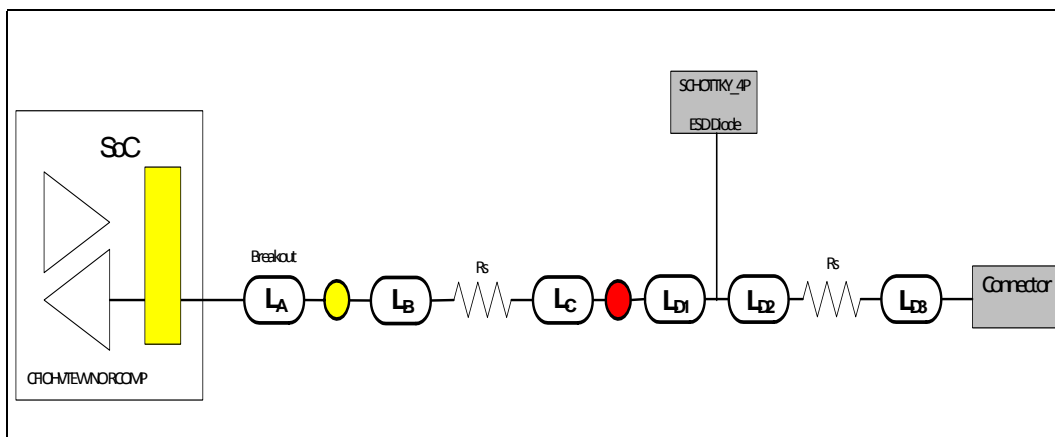
Trace Type	Stackup (MS/SL/DSL)	Units	Trace Width (W)	Minimum Spacing (S)
Microstrip	MS	mils	4	12

**Note:** The main route segments (M) of the asynchronous signals listed below are expected to follow the spacings mentioned in the table above while break-in (BI) and break-out (BO) segments are expected to have 4 mils spacing to adjacent signals.

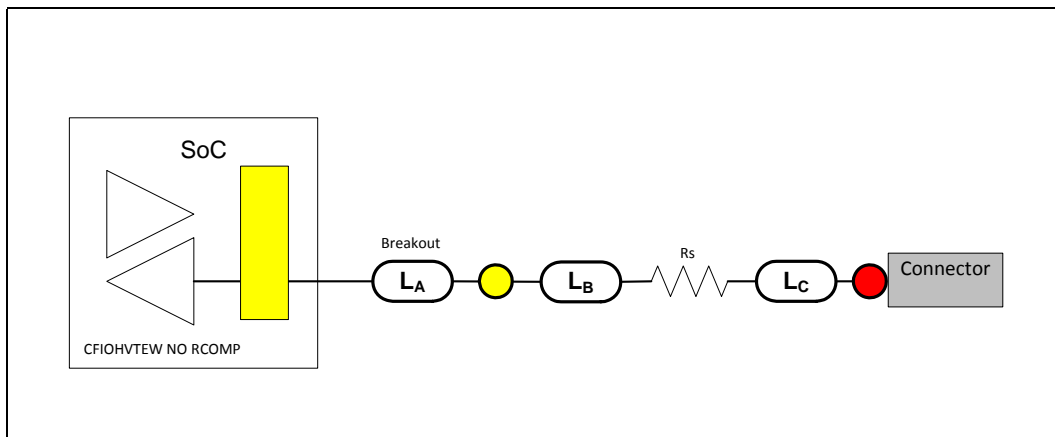
### 13.4 General GPIO Topology Guidelines

This section describes the layout recommendations for GPIO signals [7:0].

**Figure 46. Example GPIO[7:0] Topology level shifted Guideline**



**Figure 47. Generic GPIO[7:0] Topology Guideline**



**Table 50. GPIO[7:0]I General Routing Guideline (Sheet 1 of 2)**

	Breakout			
PCB Routing Layer(s) Optional	4 Layer	4 Layer	4 Layer	4 Layer
Transmission Line Segment	LA	LB	LC	LD1/LD2/LD3



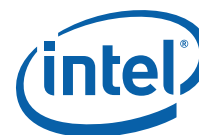
Table 50. GPIO[7:0]I General Routing Guideline (Sheet 2 of 2)

Routing Layer (Microstrip / Stripline / Dual Stripline)	MS	MS	MS	MS
Characteristic Impedance (Single-ended)	50 $\Omega$ +/- 15%			
Trace Width (w)	4.2 mil	4.2 mil	4.2 mil	4.2 mil
Trace Spacing(S2): Between GPIO Signals	4.2 mil	10 mil	10 mil	10 mil
Trace Spacing(S3): Between GPIO and other signals	4.2 mil	10 mil	10 mil	10 mil
Trace Segment Length	0.5"	min = 0.2" max = 0.8"	min = 0.1" max = 2.5"	0.25" max

Stub length	as short as possible
Number of vias	2 via
Rs	33 ohm +/- 1%
Reference Plane	Solid Ground Reference

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## 14.0 Platform Power Delivery Requirements

This chapter provides the recommended way to power up the Intel® Quark SoC X1000 from the platform. It is assumed the platform provides a single input voltage (5v) from which we derive three primary platform voltages (1.0v, 3.3v, and 1.5v). Each of these primary platform voltages are split and subsequently enabled in a specific sequence to ensure proper SoC functioning.

The platform power rails can be categorized based on S5, S3 and S0 power domains on the Intel® Quark SoC X1000.

**Table 51. Recommended Platform Power Delivery**

Primary Platform Voltage	Derivative Voltage	Derived from	Controlled by	Power-up Sequence
3.3V	V3P3_S5	Vin (5V)	Platform Power up	1
1.0V	V1P0_S5	Vin (5V)	Supply: V3P3_S5	2
1.5V	V1P5_S5	Vin (5V)	Supply: V1P0_S5	3
SoC i/p: S5_PGOOD				
3.3V	V3P3_S3	V3P3_S5	SoC o/p: S3_3V3_EN	4
1.0V	V1P0_S3_IVR	V3P3_S3	SoC internal PMU	5
1.5V	V1P5_S3	V1P5_S5	SoC o/p: S3_1V5_EN	6
SoC i/p: S3_PGOOD				
3.3V	V3P3_S0	V3P3_S5	SoC o/p: S0_3V3_EN	7
1.0V	V1P0_S0	V1P0_S5	SoC o/p: S0_1V0_EN	8
SoC i/p: PG_V1P0_S0				
1.5V	V1P5_S0	V1P5_S5	SoC o/p: S0_1V5_EN	9
SoC i/p: S0_PGOOD				

**Notes:**

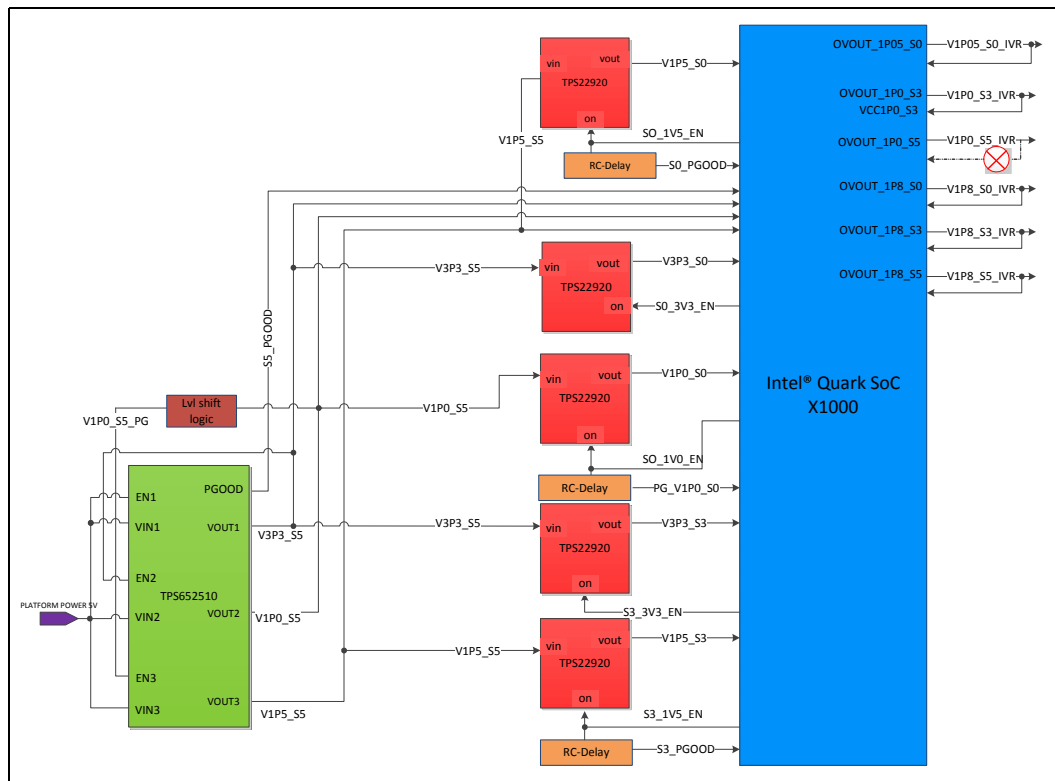
1. RED: S5 power domain
2. GREEN: S3 power domain
3. BLUE: S0 power domain
4. SoC o/p: Output handshake signal from SoC
5. SoC i/p: Input handshake signal into the SoC
6. Internal PMU: On die power management unit

S5 is the first power domain to ramp up, then S3 and subsequently the S0 power domain. 4 voltage levels exist within each power domain namely 3.3V, 1.5V, 1.8V and 1.0V. The 3.3V, 1.5V and 1.0V power rails are powered from an external power source (External to the Quark X1000 SoC on the platform). 1.8V on all 3 power domains are powered internally from on-die LDOs. V1P0\_S3 is an exception which is powered from an internal on-chip LDO.

All internal supply voltages are brought out of the SoC package and looped back-in on the platform (Refer to OVOUT\_<name> in Figure 48). This allows the system designer to disconnect the internal LDO in certain cases and supply the rail with an external voltage rail. Figure 48 illustrates the recommended platform power delivery.

Note: Figure 48 is only a block diagram and should not be treated as schematic. Refer to the Intel® Quark SoC X1000 reference design schematics for the full implementation.

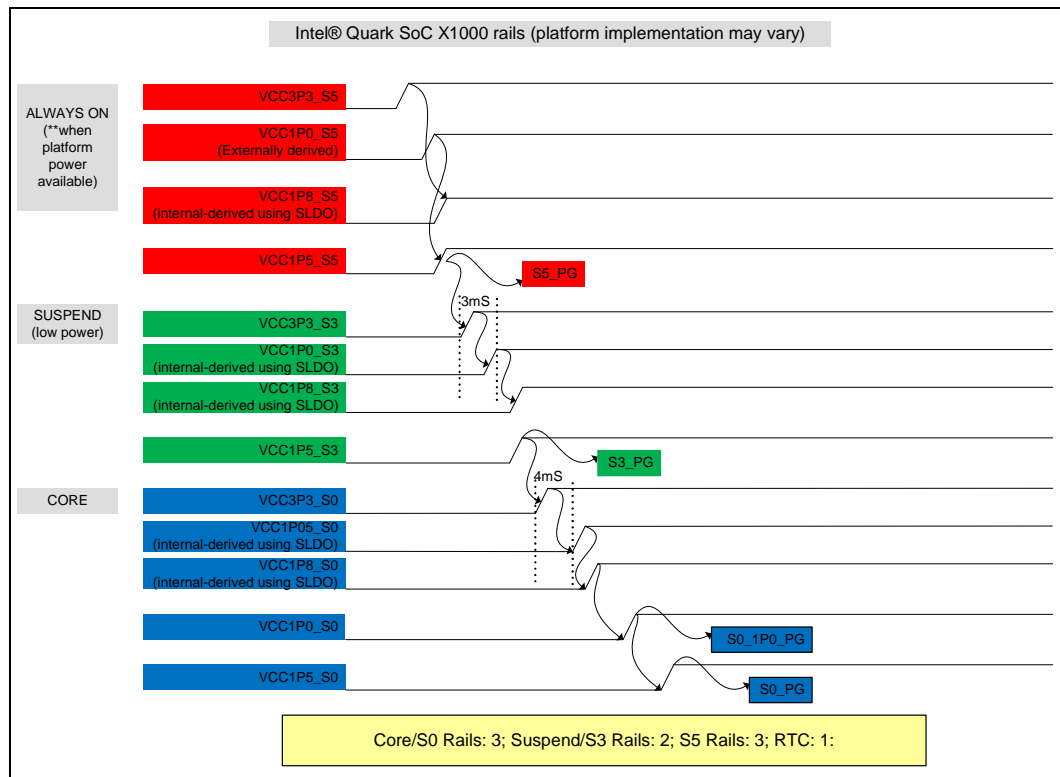
Figure 48. Intel® Galileo Platform Power Delivery



The power-up sequence specified in Table 51 is described in detail with Figure 49. At each step after the S5\_PG signal asserts, the Intel® Quark SoC X1000 internal power management block enables the subsequent power rails through a process of handshaking. These enable signals are utilized on the platform to control the FET switches which control the S3 and S0 power rails. Power good signals are needed by the Intel® Quark SoC X1000 power management unit at each power domain boundary crossing.



Figure 49. Intel® Quark SoC X1000 Power-up Sequence



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## 15.0 Platform Reset Considerations

### 15.1 Platform Reset General Introduction

#### 15.1.1 Description

Platform reset signals is a group of reset signals that control power on sequence, power management, and provide proper reset to all components on the platform. This chapter provides detailed guideline on how to generate and use platform reset signal to ensure functionality of the platform.

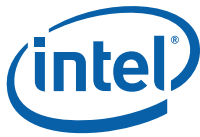
### 15.2 Signal Description

#### 15.2.1 Signal Groups

Signals listed in [Table 52](#) are identified as platform reset signals from the SoC.

**Table 52. Platform Reset Signals**

Group	Signal Name	Pin	Description
Power Management	platform_S5_pwrok	I_2PAD	Platform S5 power is okay
	platform_S3_pwrok	S3_PG	Platform S3 power is okay
	platform_S0_1P0_pwrok	S0_1P0_PG	Platform S0 power for 1.0v is okay
	platform_S0_1P5_pwrok	S0_PG	Platform S0 power for 1.5 is okay
	DRAMPWROK	ODRAM_PWROK	DRAM Power OK
	PMC_V1P0_S0_EN	S0_1V0_EN	Voltage enable for S0 v1.0 rail
	PMC_V1P5_S0_EN	S0_1V5_EN	Voltage enable for S0 v1.5 rail
	PMC_V3P3_S0_EN	S0_3V3_EN	Voltage enable for S0 v3.3 rail
	PMC_V1P5_S3_EN	S3_1V5_EN	Voltage enable for S3 v1.5 rail
	PMC_V3P3_S3_EN	S3_3V3_EN	Voltage enable for S3 v3.3 rail
	Power Management	PWRBTN#	PWR_BTN
RSTBTN#		RESET_BTN	Reset Button



## 15.3 Additional Guidelines

### 15.3.1 PMC\_V3P3\_S0\_EN# Usage Model

PMC\_V3P3\_S0\_EN# It is used primary to control platform V3P3 VR so that it will enter a more power efficient mode outside S0. It may also be used to power off all non-critical components outside the S0 state. This signal should be connected to a VR controller to enter low power mode.

### 15.3.2 PMC\_V1P5\_S0\_EN# Usage Model

PMC\_V1P5\_S0\_EN# It is used to power off all non-critical 1.5V components when not in the S0 state.

### 15.3.3 PMC\_V1P0\_S0\_EN# Usage Model

PMC\_V1P0\_S0\_EN# It is used to power off the 1.0v domain and other non-critical components outside the S0 state.

*Note:* For the S0 state to be in a stable power state all S0 rail enables must be active, in addition to the S3 rail enables.

### 15.3.4 PMC\_V3P3\_S3\_EN# Usage Model

PMC\_V3P3\_S3\_EN# It is used primary to control platform V3P3 VR so that it will enter a more power efficient mode outside S3.

### 15.3.5 PMC\_V1P5\_S3\_EN# Usage Model

PMC\_V1P5\_S0\_EN# It is used to power off all non-critical 1.5V components when not in the S3 state.

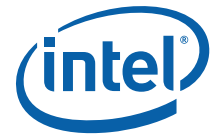
*Note:* For the S3 state to be in a stable power state all S3 rail enables must be active.

### 15.3.6 PWRBTN# Usage Model

The Power Button signal (PWRBTN#) on the Intel® Quark SoC X1000 can be connected directly to the power button on the system's front panel header. When system power button is pressed, PWRBTN# should be pulled low. The SoC has 2.6 ms of internal debounce logic on this pin, external debouncing circuit is not required. Alternatively where a front panel button is not required the PWRBTN can be tied low which results in the SoC auto booting once power is applied in S5.

### 15.3.7 RSTBTN# Usage Model

The Reset Button signal (RSTBTN#) on SoC can be connected directly to the reset button on the system's front panel header. When system reset button is pressed, RSTBTN# should be pulled low. The SoC has 2.6 ms of internal debounce logic on this pin, external debouncing circuit is not required. This button has several functions dependent on system state. If in S3 sleep a RSTBTN press will result in the SOC waking from S3 to S0. If in S0 a RSTBTN press will result in the SOC performing a WARM reset.

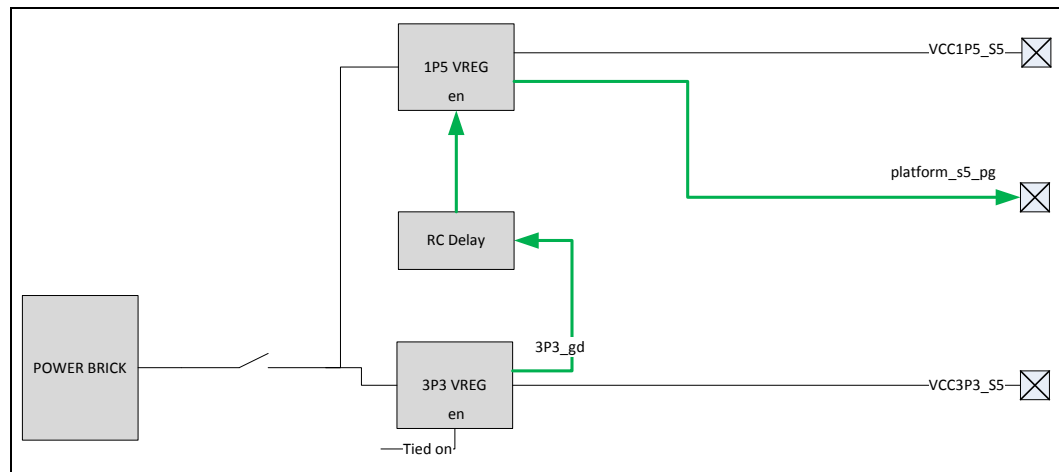


### 15.3.8 Power-well Isolation Control Signal Requirements

### 15.3.9 platform\_s5\_pwrok Generation

The platform\_s5\_pwrok signal is generated from the platform regulator V1P5 or equivalent detection logic. The signal should be generated based on the v1p5 rail achieving 90% of its nominal value

Figure 50. platform\_s5\_pwrok generation



### 15.3.10 platform\_S3\_pwrok Generation

The platform\_s3\_pwrok signal is generated from the platform power switched S3 V1P5 or equivalent detection logic. The signal should be generated based on the S3 v1p5 rail achieving 90% of its nominal value. The S3 v3p3 and v1p5 rails are enabled by SoC via the v3p3\_s3\_en and v1p5\_s3\_en sequence.

### 15.3.11 platform\_S0\_1P0\_pwrok Generation

The platform\_s0\_1p0\_pwrok signal is generated from the platform regulator S0 V1P0 or equivalent detection logic. The signal should be generated based on the S0 v1p0 rail achieving 90% of its nominal value. The v1p0 rail is enabled by SoC via the v1p0\_s0\_en.

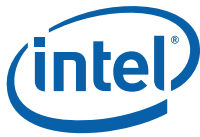
### 15.3.12 platform\_S0\_1P5\_pwrok Generation

The platform\_s0\_1p5\_pwrok signal is generated from the platform power switched S0 V1P5 or equivalent detection logic. The signal should be generated based on the S0 v1p5 rail achieving 90% of its nominal value. The S0 v3p3 and v1p5 rails are enabled by SoC via the v3p3\_s0\_en and v1p5\_s0\_en sequence.

### 15.3.13 Glue Logic Device

Glue Logic Devices are available from various vendors to provide an ASIC component that integrates miscellaneous platform logic into a single chip.

Contact your preferred vendor for available glue logic solution.

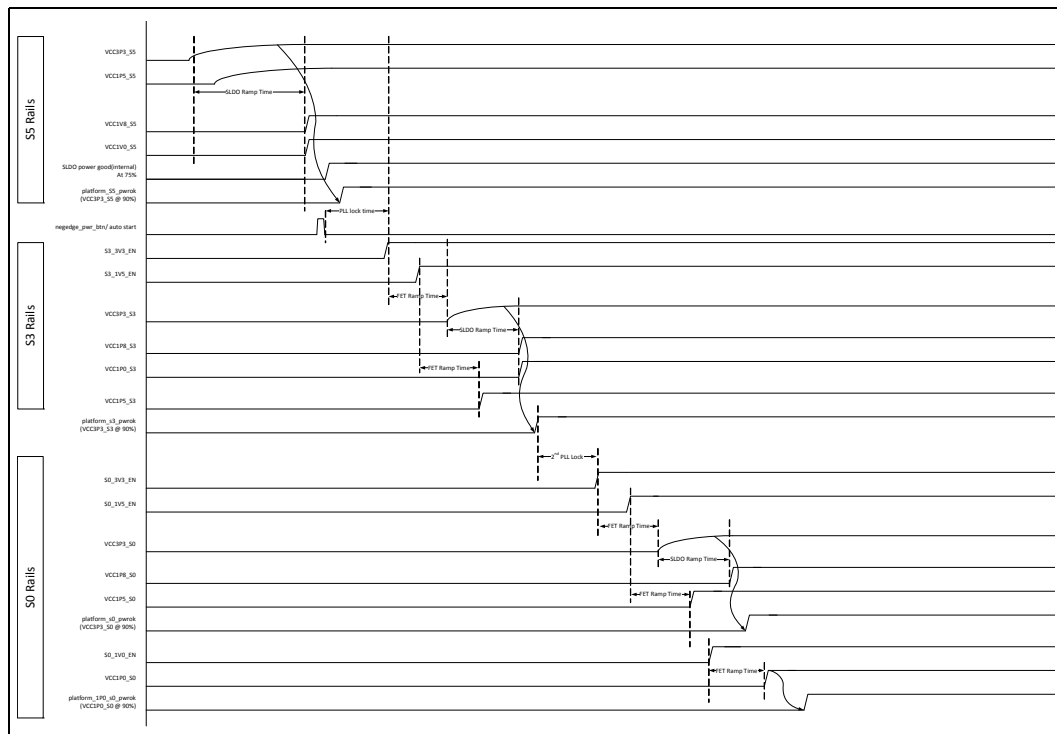


### 15.3.14 Additional Power Sequencing Considerations

It is possible that on rare occasions, wake events can cause the system to immediately wake after entering in S3 power state. In such circumstances it is possible that the SoC will generate the same duration pulse widths on the v3p3\_s0\_en, v1p5\_s0\_en and v1p0\_s0\_en as during normal cold boot. Care should be taken during the platform design to evaluate and account for such events in terms of VR design, power good circuitry design, and overall platform power sequencing in order to ensure timing specifications related to power sequencing are not violated.

### 15.3.15 Power Sequence Timing Diagram

Figure 51. Power Sequence Timing





## 16.0 Critical Low Speed Signals Design Guidelines

### 16.1 Critical Low Speed Signals General Introduction

#### 16.1.1 Description

Critical Low Speed Signals are identified as critical input signals from the Intel® Quark SoC X1000 that are low frequency but have huge impact to system functionality or stability. Glitches on these signals may cause system to behave in unpredicted manners or cause unpredicted system shutdown or reset. Although these are low speed signals in nature, glitches may be induced or coupled from nearby high speed signals. Therefore it is important to keep these signals clean from any potential sources of glitches on the platform.

### 16.2 Critical Low Speed Signal Descriptions

#### 16.2.1 Signals Group

Signals listed in [Table 53](#) below are identified as critical input signals from the Intel® Quark SoC X1000 that must be guaranteed glitch free all the time.

**Table 53. Critical Signals**

Group	Signal Name	Description
RTC	RTCRST_B	<b>RTC Reset:</b> When asserted, this signal resets register bits in the RTC well.
Power Management	S5_PG	<b>Power OK:</b> When asserted, PWROK is an indication to the SoC that all of its S5 power rails have been stable for 10 ms. S5_PG can be driven asynchronously.
Power Management	S3_PG	<b>Power OK:</b> When asserted, indicates that power to the S3 power rails are stable.
Power Management	S0_1P0_PG	<b>Power OK:</b> When asserted, indicates that power to the S0 1P0v power rail is stable.
Power Management	S0_PGGOOD	<b>Power OK:</b> When asserted, indicates that power to the S0 1P5v power rail is stable.
Power Management	PWR_BTN	<b>Power Button:</b> The Power Button will indicate to the system a request to go to S0. If the system is already in a sleep state S3, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Forced shutdown is only active in the S0 state.
Power Management	WAKE_B	<b>PCI Express* Wake Event:</b> Sideband wake signal on PCI Express asserted by components requesting wake up.



### 16.3 Additional Guidelines

All critical signals must stay away from potential glitch or noise sources on the platform. It is recommended to keep all critical signal traces a minimum of 15 mils away from any clock or high speed differential signals with > 4V/ns edge rate, to avoid glitches from crosstalk.

Table 54. Critical Signals Routing Summary

Parameter	Stackup (MS/SL/DSL)	Units	Routing Recommendation
Spacing	MS	mils	15mils

Experiment data shows that certain signals have shown high sensitivity to specific frequencies. Routing those signals near to the frequency source will increase the glitches due crosstalk. The relationship of each signals with the frequency it is sensitive to, is listed in Table 55. Designer should try to avoid routing a signal next to the sensitive frequency and the harmonics of its sensitive frequency. If this cannot be avoided, it should be kept a minimal of 15 mils from the respective signal trace.

Table 55. Frequency Sensitivity

Signal Name	Frequency to Avoid
PWRBTN#	25 MHz
WAKE#	12.5 MHz

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## 17.0 Electromagnetic Interference

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### 17.1 Electromagnetic Interference (EMI) General Introduction

#### 17.1.1 Description

The main component of EMI is a radiated electromagnetic wave, which consists of both electric (E-fields) and magnetic (H-fields) waves traveling together and oriented perpendicular to each other. E-fields are created by voltage potentials while H-fields are created by current flow. If a dynamic E-field is present then there must be a corresponding dynamic H-field, and vice versa. Motherboards with fast processors will generate high frequency E and H fields from currents and voltages present in the component silicon and signal traces.

Prevention and containment minimize E and H field emissions from a system. Prevention minimizes the ability of the motherboard to generate EMI fields. Containment contains radiated energy within the chassis.

Careful consideration of board layout, trace routing and grounding may significantly reduce the motherboards radiated emissions and make the chassis design easier.

### 17.2 Exercising the System for EMC Testing

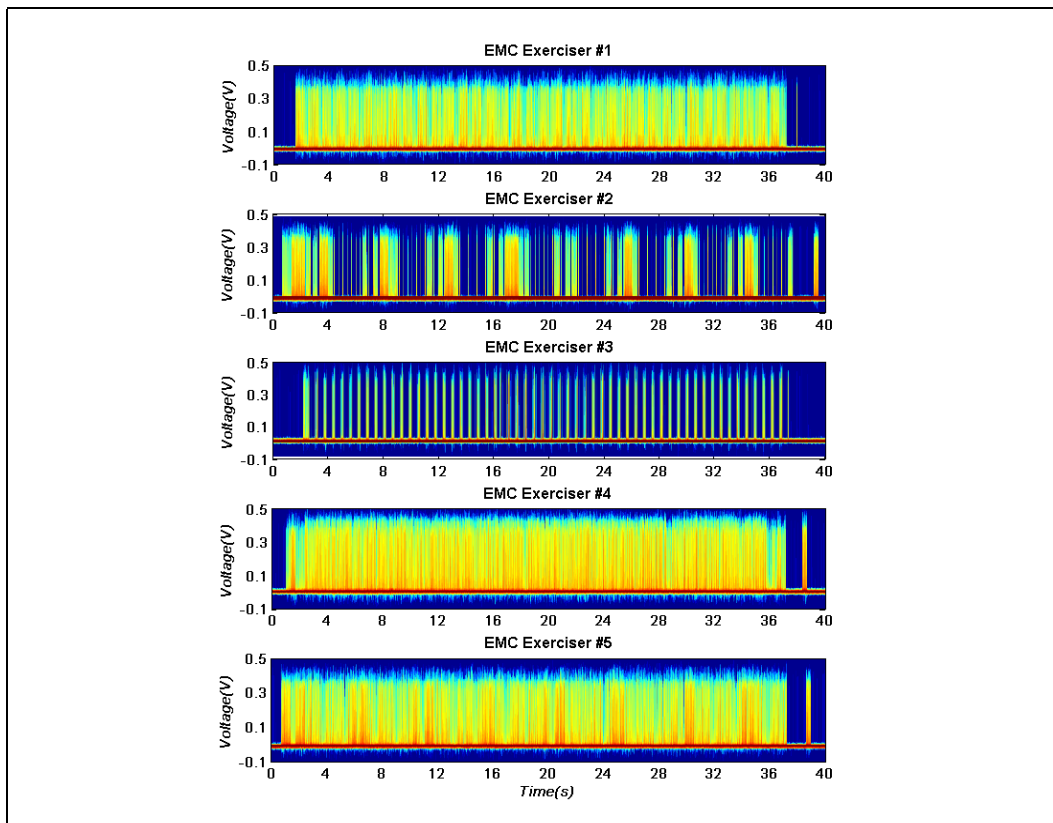
Computing platform regulatory testing utilizes software to exercise all parts of the computer thereby generating emissions to gauge EMC compliance. Regulatory standards provide general guidance for Information Technology Equipment (ITE) operating conditions including a description of the exercising software operation but not to the extent necessary to have repeatability across the industry.

Experimentation using a combination of different OEM and commercial exercisers have shown a significant deviation of the EMI signature on the same system. Key variables of the software have been identified that control the EMI signature. These variables are not addressed by the regulatory standard and are implemented at the discretion of the software developer. The attributes that directly impact the EMI signature are:

- **Data Sequence:** Write-Read-Erase sequence ensures data is not cached which creates period of inactivity.
- **Data Pattern:** Determines the spectral content as a function of the data-rate clock.
- **File Size:** Sets the size of the file on the data device where the data pattern is written and read from. This will indirectly impact the duty cycle of the write-read-erase sequence and period.
- **Block Size:** Sets the size of the data block where the data is written and read from. This will indirectly impact the duty cycle of the write-read-erase sequence and period.

[Figure 52](#) is a time domain capture of the bus activity using each exerciser. While the software interface is virtually identical for each exerciser, it is clear what is occurring internally in the exerciser, changes the drive activity which directly correlates to EMI levels. edges. The higher the activity seen on the bus, the higher the EMI levels are.

Figure 52. Time Domain Capture of Exerciser Operation



It is recommended to use a write-read-erase sequence with a random data pattern. While a repeated pattern is very reproducible, it will produce far worse and unrealistic EMI levels than a typical real-world application. Applying the video scrolling H pattern to data devices is considered a repeated pattern and is not required. The exercising software should be flexible to allow the user to manually set the file and block sizes. The time between the write and read cycle is based on the file size. Smaller block sizes will cause higher bus and drive activity. It is recommended to set a very large file size with a very small block size to maximize emissions from the PC.



## 17.3 EMI Source

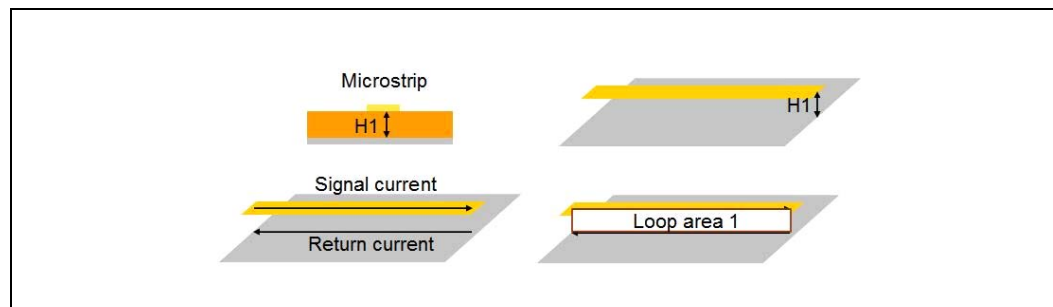
### 17.3.1 Current Loop Radiation

Current loop radiation is formed by the forward current and return current. For example, the current loop of signals travelling on a microstrip line is shown in the following figure. The current traveling on the trace is the forward current. The current traveling on the ground plane is the return current. The forward and return currents then form a current loop in between the trace and ground plane. Current loops, like magnetic dipoles, emit signals. The emission intensity is proportional to the current strength and the loop area. Therefore, minimizing the loop area is a key to mitigate EMI.

Two ways to keep the microstrip-line current loop area small:

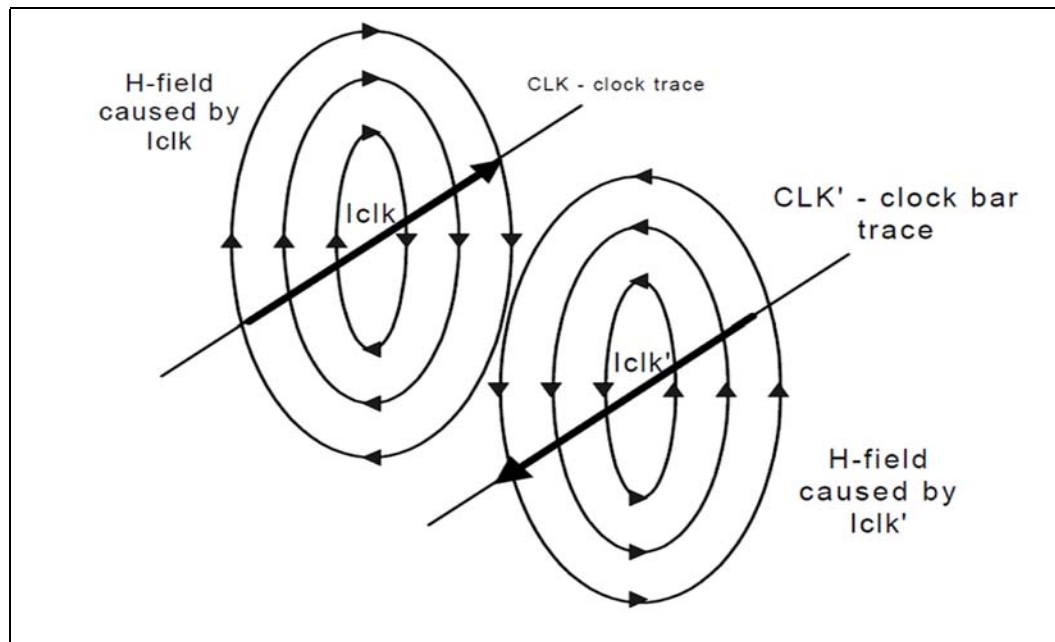
- Keep the height of the dielectric in between the trace and ground plane as small as possible.
- Keep the length of the trace as short as possible. In other words, route the signals short.

**Figure 53. Current Loop Radiation of a Transmission Line**



Similar concepts can be applied to striplines and dual-striplines. A stripline or dual-stripline usually emits less than a microstrip line does. It is because a stripline or dual-stripline forms two current loops in opposite directions: clockwise and counterclockwise. These two loops more or less cancel their emission each other.

A differential line is a good example of current loop radiation cancellation. A differential line is composed of two adjacent traces. Therefore, the current loop from one trace is very similar to the loop from the other. Since the current traveling on these traces are in opposite direction. As a result, the emissions caused by these two loops cancel each other. Please note that the cancellation is maximum when forward and return currents are balanced. Unbalanced current levels induce common mode radiation introduced in [Section 17.3.3](#).

**Figure 54. Radiation Cancellation of a Differential Line**


### 17.3.2 Voltage Regulator Module Current Loop Radiation

The noise from voltage regulator module (VRM) is typically around 50~300MHz. The two noise peaks at 125 and 250 MHz shown in [Figure 55](#) are an example. VRM noise can cause both signal integrity (SI) and EMI issues (see [Figure 56](#)) through the same or different coupling paths. Besides the coupling paths elimination, the issues can be resolved effectively by mitigating VRM noise from the source. [Figure 57](#) shows a simplified VRM circuit. The VRM EMI noise can be detrimental when its harmonics coincide with the resonant frequency of the input decoupling path which encompasses input decoupling capacitors and the top and bottom transistors. A practical way to mitigate the VRM noise without sacrificing VR efficiency is to have minimal parasitic PCB inductance of the current loop indicated above. Several good layout practices are listed in the followings: Have a solid ground plane immediately underneath the VRM circuit and connect the VRM ground to the solid ground plane through vias. These Vias should be placed close to the low-side FET.

- Place the decoupling capacitors very close to the top transistor. The ground pin of the capacitors should be connected to the solid ground plane right underneath.
- Use at least two decoupling capacitors to reduce overall parasitic inductance from the capacitors themselves.
- If transistors are placed at different layers, ground vias should be placed close to the phase node vias.

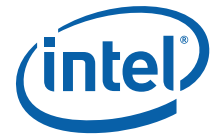


Figure 55. An Example of VR EMI Noise

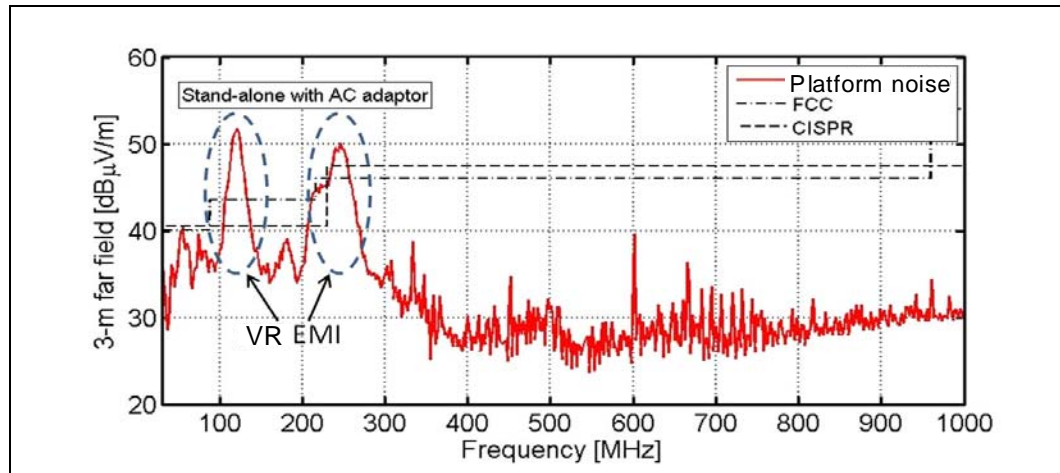


Figure 56. VR Noise Can Result In Both SI and EMI Issues

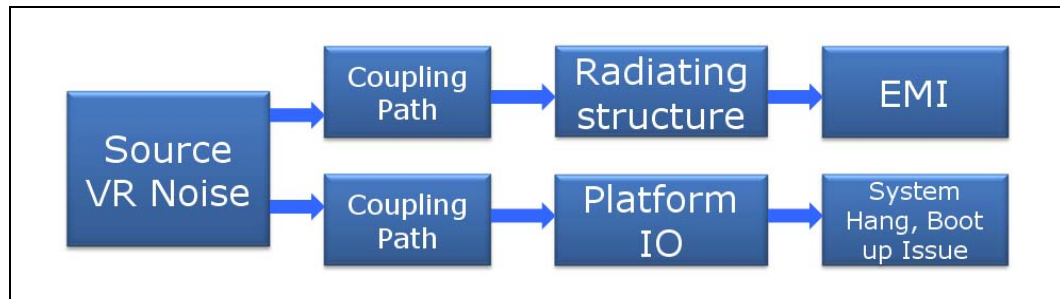
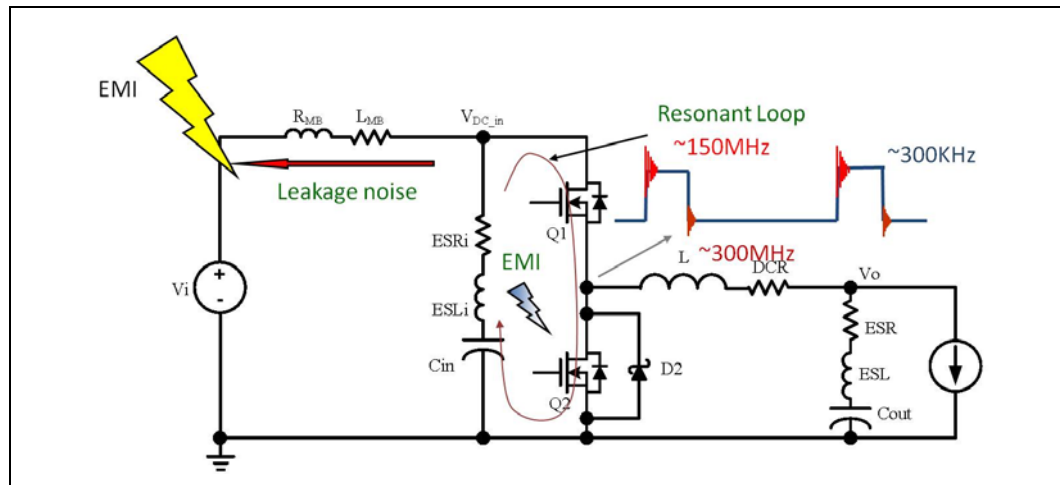
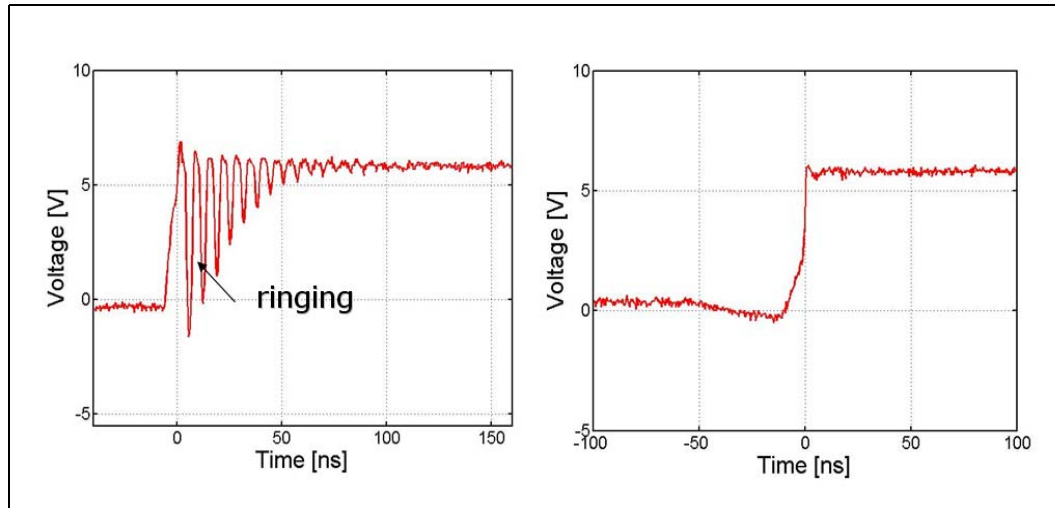


Figure 57. Simplified Voltage Regulator Module Circuit and VRM EMI Noise



It is also found that the EMI noise is correlated with the ringing at the phase node ( $V_x$ ). A way to mitigate the ringing amplitude is to slightly increase the gate resistance of Q1 and/or Q2. However, it should be aware that increasing gate resistance impacts power efficiency of the VRM circuit.

**Figure 58. The Vx Ripples with/without Gate Resistors (Left: without gate resistor/ Right: with gate resistor)**



Besides the 50 to 300MHz EMI noise, the hundreds kHz switching noise can result in signal integrity issues if the noise is coupled to IO nets in proximity. It is critical to trap the noise within the input loop and minimize the noise propagation. Several design methods can be tried to reduce the switching noise (ripple): increase the total input capacitance value, mix the power and Vss via at the phase node, and minimize the size of the phase noise.

### 17.3.3 Common Mode Radiation

Common mode radiation happens when current travels through an IO cable or when signals are coupled to a heat sink (heat spreader) or power/ground planes. Cable, metal planes, and heat sink then become antennas that radiate. If the antenna is electrically small, it can be an electric dipole (for example IO cable or emission below 300 MHz). Its radiation intensity is proportional to the length of the antenna and signal frequency. However, the intensity becomes the maximum when the signal frequency reaches the antenna resonant frequency. Heat sink radiation and power/ground plane resonances are examples. Heat sink radiation and power/ground plane resonances are catching more attention recently because of the increasing signal speed (frequency).

Another example of common mode radiation is due to the signal timing skew on a differential line. The skew causes the unbalance of the currents traveling on the traces. As a result, a common mode current is induced and the emission becomes much higher. Besides the timing skew, any unbalance designs in the PCB including the non-homogeneous PCB material such as FR-4 can result in common mode current on a differential pair. Therefore, differential routings, especially USB2, should follow the EMC design rules mentioned in the following sections.

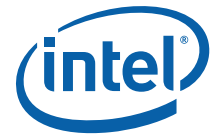
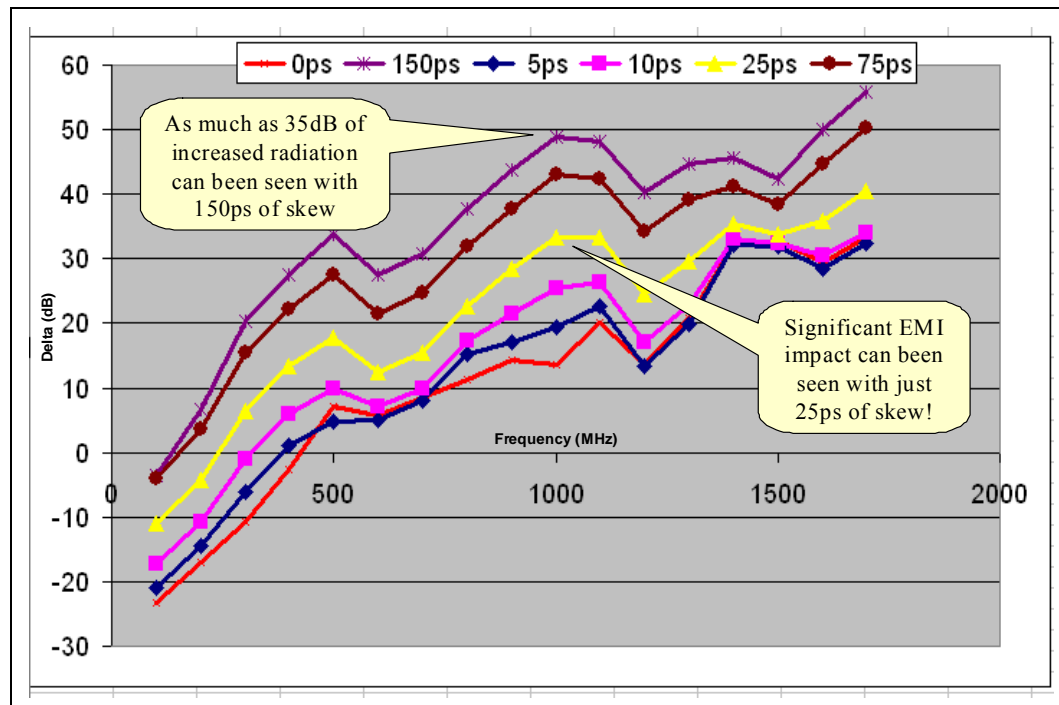


Figure 59. Emission from a Differential line with Various Skews

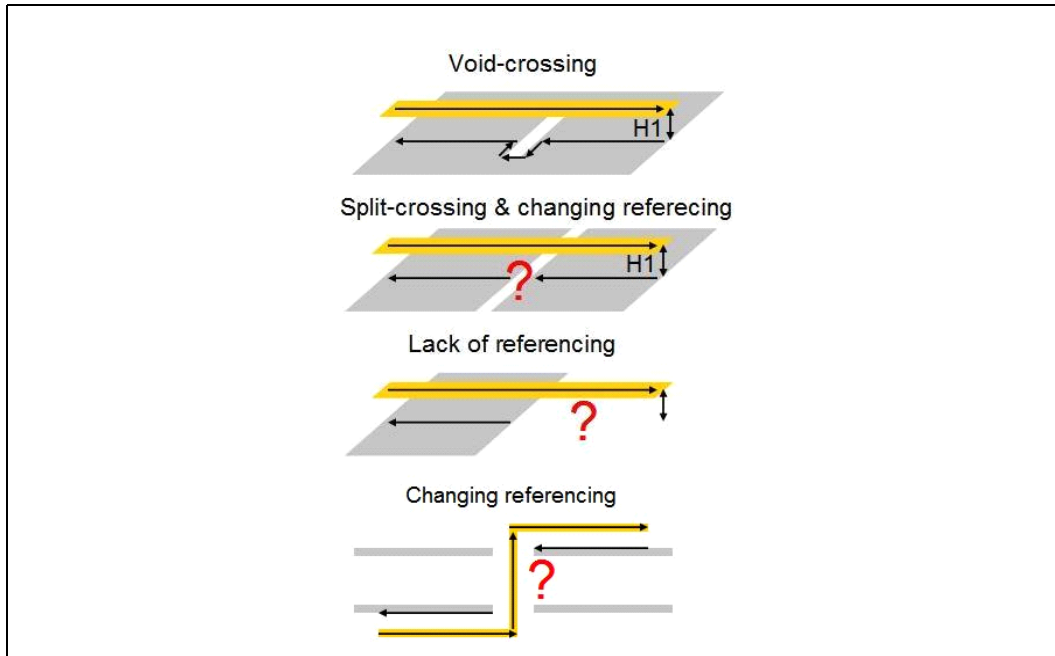


## 17.4 EMI Optimization Guideline

### 17.4.1 Avoid Changing Referencing, Lack of Referencing, Void-crossing, and Split-crossing

Lack of referencing, reference changing, void-crossing, and split-crossing shown are common practices in order to accommodate all signals and power networks. However, they cause much stronger radiation due to the greatly increased current loop area. Avoid these layout practices.

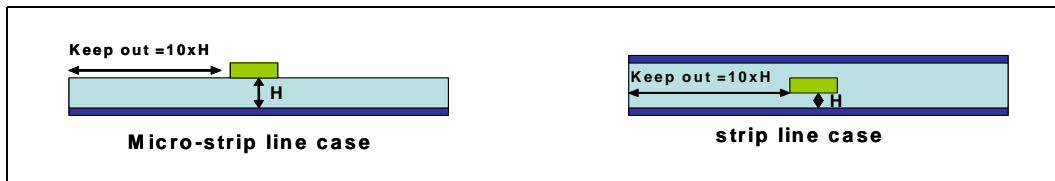
**Figure 60. Changing Referencing, Lack of Referencing, Void-crossing, and Split-crossing are Not Recommended**



### 17.4.2 Avoid Signal Traces Too Close to the Edges of Planes

Signal traces routed too close to the edges of referencing planes excite edge radiations. It is because the return current distribution on the referencing planes are terminated by the edges. For acceptable radiation have  $10 \times H$  keep-out area. Edge-to-trace distance should be 10 times greater than then dielectric height ( $H$ ).

**Figure 61. Signal Traces Should be away from Plane Edges**



### 17.4.3 Avoid Unnecessary Traces Too Close to IO and Other Connectors

Signals couple to connectors more strongly while signal traces are routed too close to the connectors. The coupling signals then radiate through connectors and the attached cables. Increasing distance between traces and connectors can reduce coupling. Therefore, a  $10 \times H$  keep-out area should be applied to the connectors  $H$  is the dielectric height between signals traces and referencing planes.

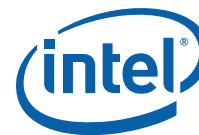
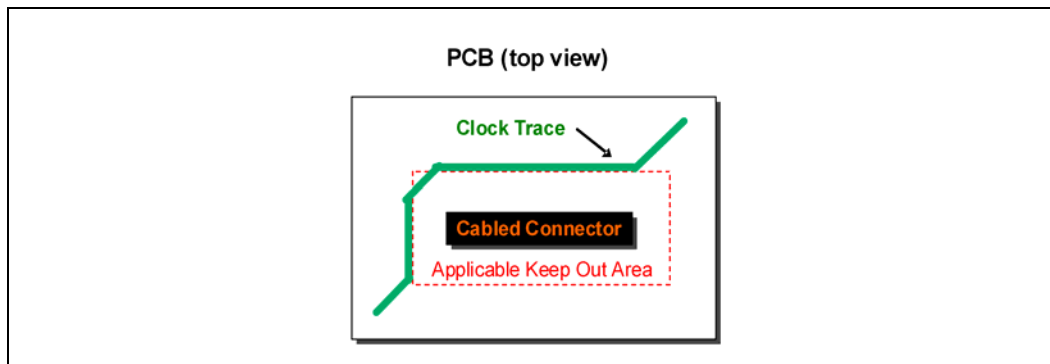


Figure 62. Keep-out Zone Determined Around IO and Other Connectors



### 17.4.4 EMI Mitigation through Stitching and Decoupling Capacitors

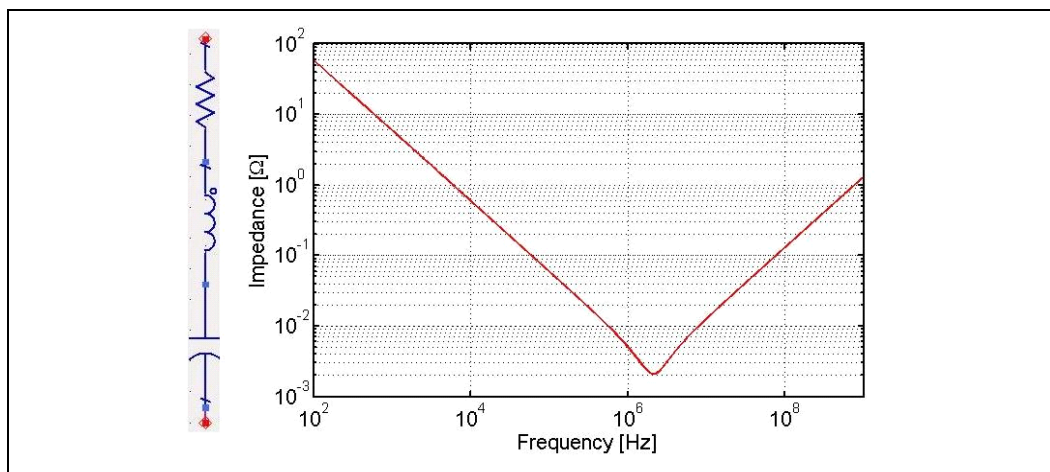
EMI emission can be mitigated with capacitors, which create low-impedance paths for signals or noises to pass through. These paths could minimize current loop areas or change plane resonant frequencies.

It is important to understand the capacitor model and its relationship with impedance. A simple capacitor model is a series of resistor (R), inductor(L), and capacitor(C). Therefore, the impedance of a capacitor can be expressed by the following equation.

$$Z(f) = R + j\left(2\pi fL - \frac{1}{2\pi fC}\right)$$

The impedance is a function of frequency. It is lowest when the frequency is at  $1/(2\pi\sqrt{LC})$ . This frequency is call the self-resonant frequency. Below this frequency, the impedance is dominated by the capacitor value. Above this frequency, the impedance is dominated by the inductor value. At this frequency, the impedance is determined by the resistor value. The self-resonant frequencies normally are below 100 MHz. As the signal and clock speeds are ever-increasing. The concerned emissions could reach above 100 MHz. The inductor impact is getting more critical. Choosing a capacitor with low inductance is important.

Figure 63. Simple Capacitor Model and an Example of Capacitor Impedance



Two main EMI mitigation methods using capacitors are introduced in the followings. They are stitching capacitor and decoupling capacitor.

### 17.4.4.1 Stitching Capacitors

Stitching capacitors are used to create return current path for signal traces with different references. Using stitching capacitors for split-crossing is one example. The separated reference planes have different voltages. They are, therefore, not able to be merged. As a result, there is no low impedance path for the return currents. The current loop becomes large and unpredictable. Connecting one or two capacitors between the two planes could provide low impedance return paths. Therefore, the new current loop is controlled.

Figure 64. Stitching Capacitors Could Create Low Impedance Path for Return Currents

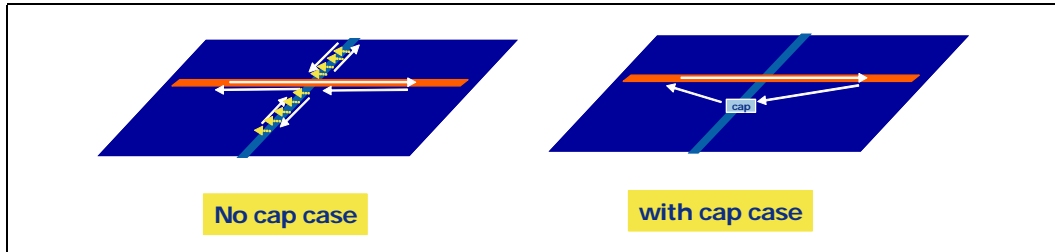


Figure 65 shows an example of stitching capacitor impact on EMI radiation. The simulated results show the different emissions of a microstrip line with a perfect referencing, a microstrip line with split-crossing, a split-crossing microstrip line with one stitching capacitor, and a split-crossing microstrip line with two stitching capacitors. It is observed that split-crossing results in much higher emission. Placing one stitching capacitor reduces emissions. Placing two stitching capacitors symmetrically to the trace greatly reduces EMI.

Stitching capacitors should be placed as close as possible to the troubled signal traces. Figure 66 shows different emissions when the stitching capacitors are placed 1-mm and 2-mm away from the trace. To maximize stitching capacitor effect:

- Two capacitors placed symmetrically to the split-crossing trace show much better mitigation than one capacitor only.
- Capacitors should be placed as close as possible to the split-crossing trace.



Figure 65. Stitching Capacitors Mitigate EMI (Simulated Results)

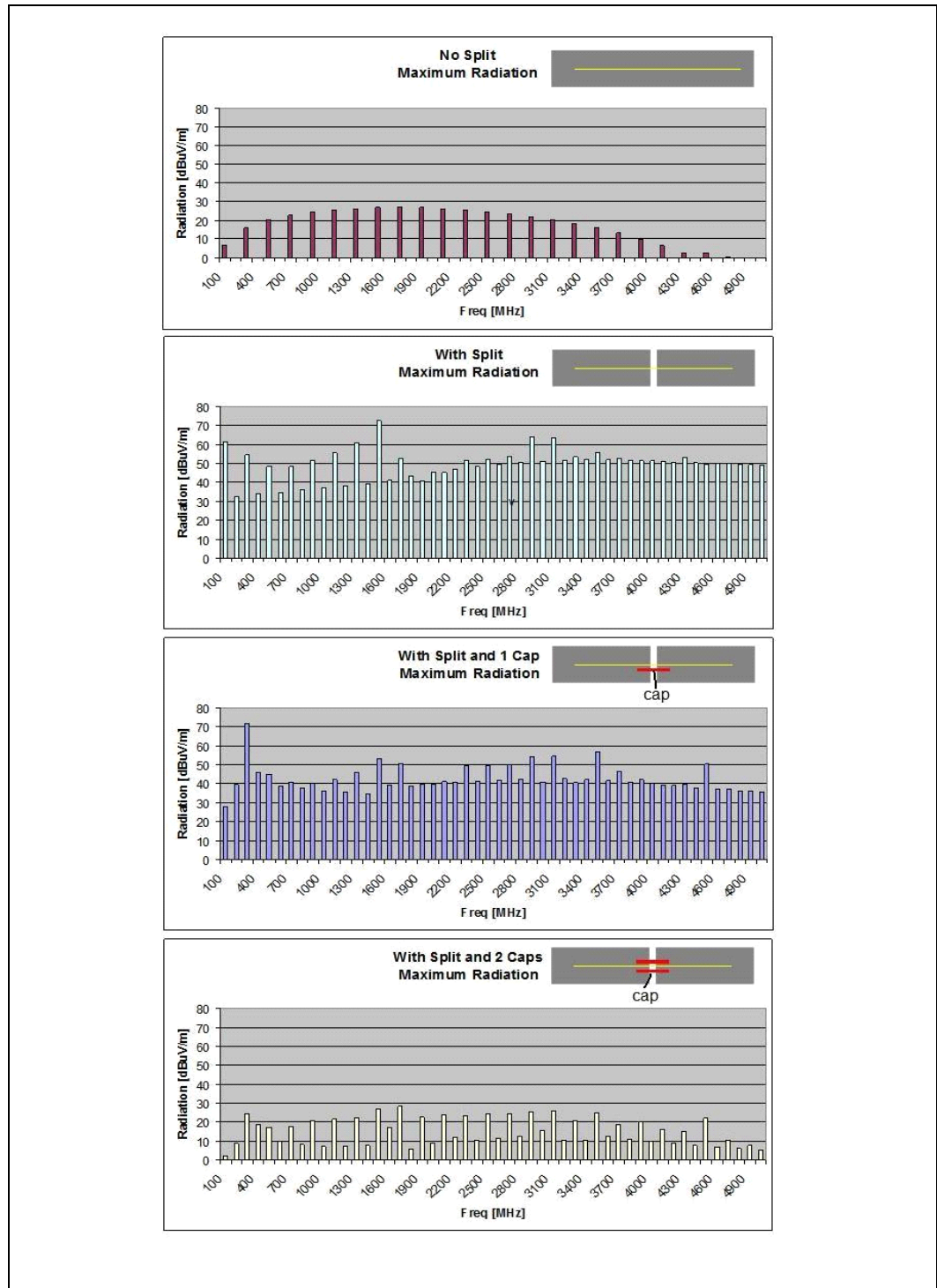
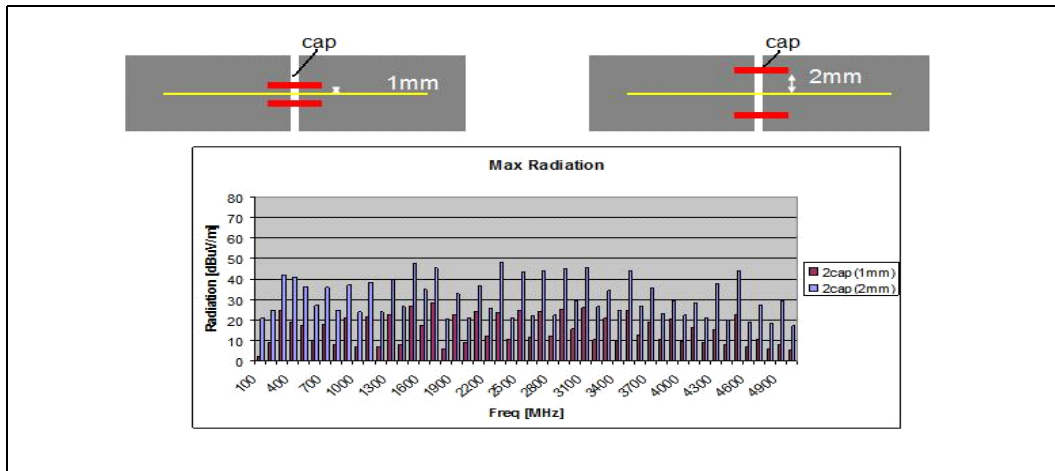


Figure 66. **Stitching Capacitors Should be Close to Traces**

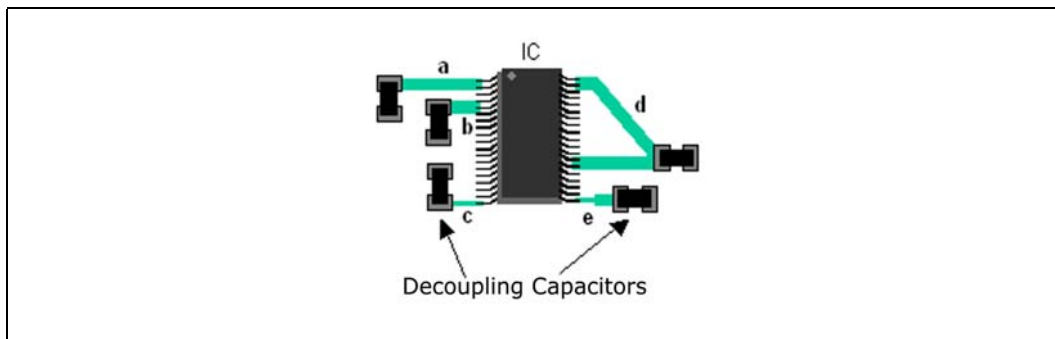


#### 17.4.4.2 Decoupling Capacitors

Decoupling capacitors are used to mitigate the noise on power rails or planes. Noise sources on power rails or planes are mainly from voltage regulators and IC chipsets. Decoupling capacitors connected between power and ground could create shorter return paths for the noise currents. In order to minimize return paths, place capacitors as close as possible to noise sources.

In “[Decoupling Capacitors Locations](#)”, option “b” is the best because the decoupling capacitor is placed closest to the IC and the wider power rail has lower inductance. “[Decoupling Capacitors with Vias](#)” shows the via locations. Vias should be placed where the traces are decoupled prior to being routed. Locations “a” and “b” are acceptable. Location “c” is not acceptable since the via is placed before the bypass capacitor. Location “d” is poor since two capacitors are tied to one via (this is not a good practice). Location “e” is poor since two capacitors are tied to one via and the via is before the capacitor (the via should be on the other side of each capacitor).

Figure 67. **Decoupling Capacitors Locations**



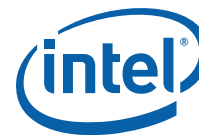
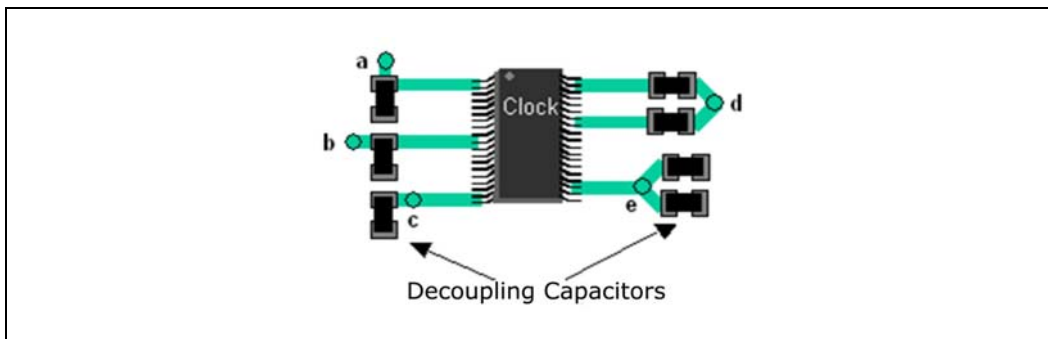
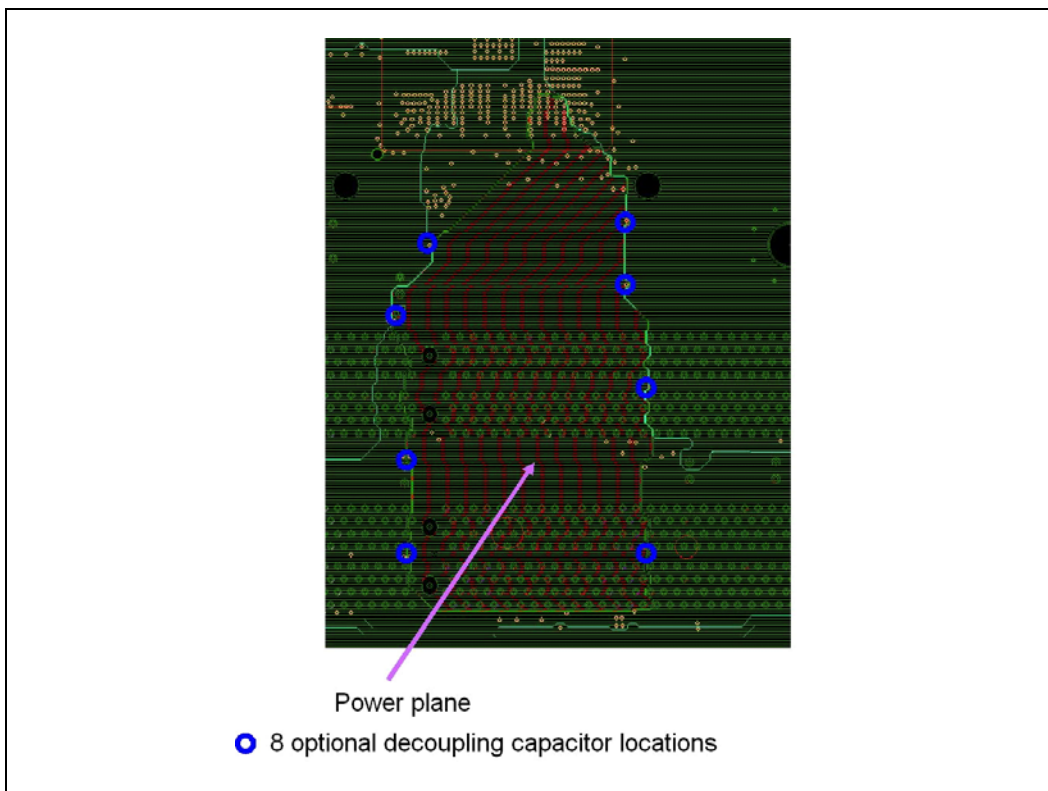


Figure 68. Decoupling Capacitors with Vias



Other noise sources are from the signal traces adjacent to power planes. Power plane could be considered as an antenna radiating noises coupled from these traces. Populating decoupling capacitors around the planes is a way of mitigation.

Figure 69. Decoupling Capacitors Around the Edges of Power Plane



## 17.4.5 Common Mode Filter

Some IO signals are differential. Differential signals are robust to EMI unless the differential signals are unbalanced.

IO differential lines result in common mode radiation. Common mode filters are generally recommended for mitigating common mode radiation. They should be placed in series with differential lines and close to IO for maximum effect.

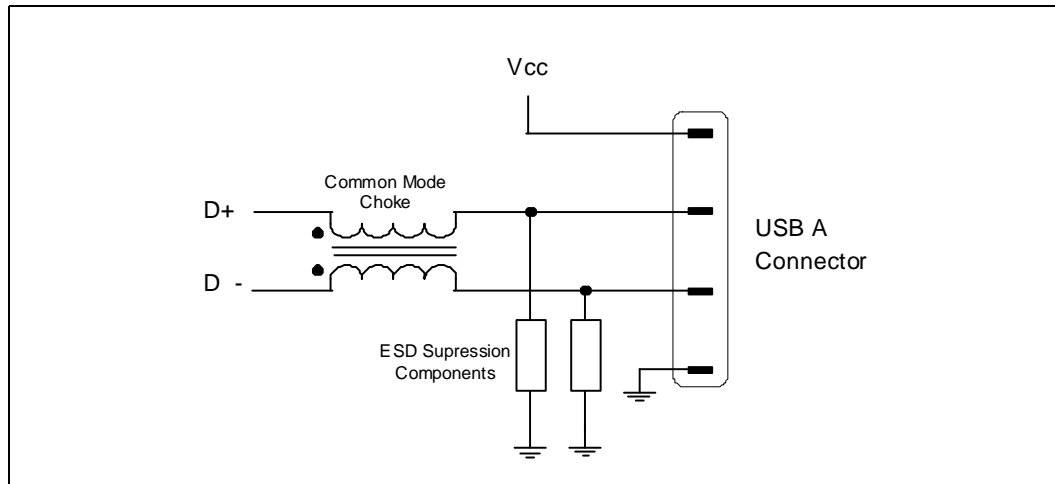
### 17.4.5.1 USB Common Mode Choke Recommendation

Intel recommends implementing a common-mode choke (CMC) footprint for each USB 2.0 pair. Please refer to [Section 17.4.6](#) for USB 2.0 common mode choke recommendations.

## 17.4.6 USB 2.0 Common Mode Chokes

Testing has shown that common mode chokes can provide required noise attenuation. A design should include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. [Figure 70](#) shows the schematic of a typical common mode choke and ESD suppression components. Place the choke as close as possible to the USB connector signal pins.

**Figure 70. USB 2.0 Common Mode Choke**



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases, the distortion will increase, so you should test the effects of the common mode choke on full speed and high-speed signal quality. Common mode chokes with a target impedance of  $80\ \Omega$  to  $90\ \Omega$  at 100 MHz generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process:

- Choose a part with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that should be suppressed.
- After obtaining a part that gives passing EMI results, the second step is to test the effect this part has on signal quality. Higher impedance common mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing



means that the signal quality must be checked for low-speed, full-speed, and high-speed USB operation.

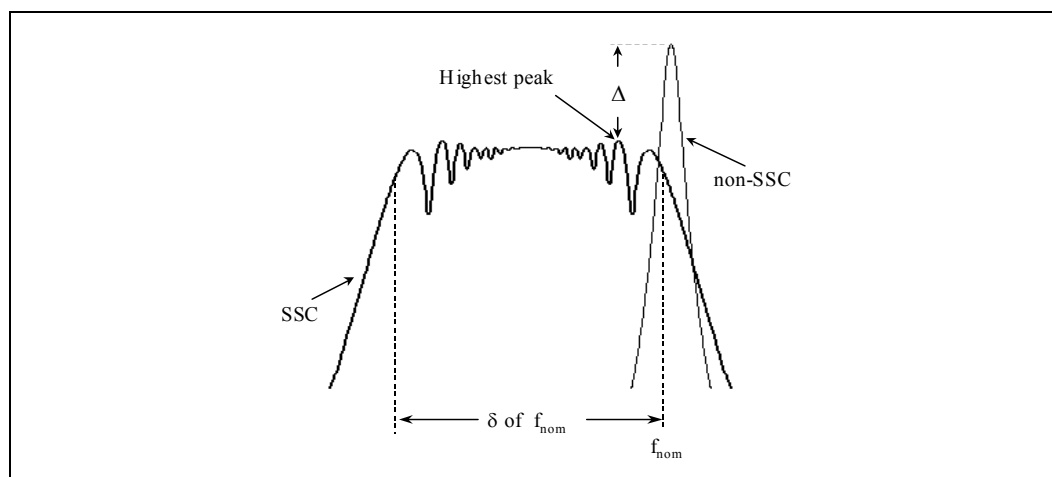
- Further common mode choke information can be found on the high-speed USB Platform Design Guides available at [www.usb.org](http://www.usb.org).

### 17.4.7 Spread Spectrum Clocking

Although clock noise is inherently narrow band in nature, there are cases where the clocks are deliberately modulated or “spread”. The most common reason for doing this is to reduce spectral peaks that might otherwise violate FCC and CE requirements for unintentional (EMI) radiation.

The spread spectrum clocking technique reduces radiated emissions by spreading the emissions over a wider frequency band. This band can be broadened, with subsequent reductions in the measured radiation levels, by slowly frequency modulating the clock over a few hundred kHz. Thus, instead of maintaining a constant system frequency, SSC modulates the clock frequency/period along a predetermined path (i.e., modulation profile) with a predetermined modulation frequency. The modulation frequency is usually selected to be larger than 30 KHz (above the audio band) while small enough not to upset the PC system’s timings.

Figure 71. Demonstration of Spread Spectrum Clocking (SSC)



Although the spread spectrum clocking (SSC) technique has been demonstrated to reduce peak radiation by approximately 8 dB and are widely applied in clocking system, clocks are still key radiation sources that cause EMI. Designers must not assume SSC clocking will eliminate EMI problems especially if the technique is not implemented correctly.

Radiated emissions are typically confined in a narrow band centered around clock frequency harmonics. By uniformly distributing the radiation over a band of a few MHz, regulatory measurement levels (in a 120 kHz bandwidth at frequencies below 1 GHz and in a 1 MHz bandwidth at frequencies above 1 GHz) will be reduced.

To conserve the minimum period requirement for bus timing, the SSC clock is modulated between  $f_{nom}$  and  $(1 - \delta)f_{nom}$  where  $f_{nom}$  is the nominal frequency for a constant-frequency clock;  $\delta$  specifies the total amount of spreading as a relative percentage of  $f_{nom}$ .

The frequency modulation in the time-domain results in a frequency-domain energy redistribution of the constant-frequency clock harmonics. The shape of the spectral energy distribution of the SSC is determined by the time-domain modulation profile, while the energy distribution width is determined by the modulation amount ( $\delta$ ). The two combined determine the amount of EMI reduction ( $\Delta$ ).

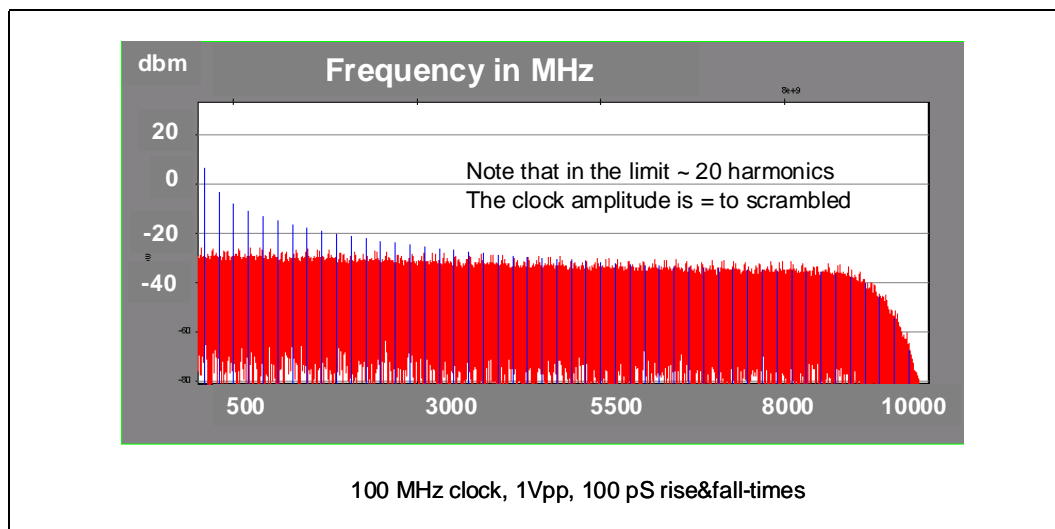
The clock frequency deviation ( $\delta$ ) is required to be at least 0.5% down-spread from the corresponding nominal frequency (+0% / -0.5%). The width of its spectral distribution is between the -3 dB roll-off points. The ratio of this width to the fundamental frequency cannot exceed 0.5%. The total power can be estimated by measuring the power density and integrating over the frequency of interest to obtain total power. Normally, clock signals are “down-spread”, that is, modulated so that all the sideband power is lower than the original center frequency. This prevents “over-clocking”, or running clocks higher than specified, a condition that might cause a system to hang.

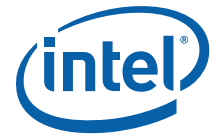
### 17.4.8 Signal Scrambling

Most EMI problems in electronic systems can be attributed to repetitive signals. In high-speed communications these repetitive signals are not limited to the clocks. For instance, data that is periodic itself can lead to an EMI problem. To minimize EMI risk due to such events, every character, except for those encoded into special symbols (K codes), and the characters that are within the training sequences are scrambled. In this way the repetitive nature of data such as 'H' patterns, as dictated by the FCC for testing of video interfaces, do not exhibit an increase in EMI over random data. Additional information on the specific scrambling algorithm used can be found in technology specifications, e.g. PCI Express base specification.

Figure 72 shows a comparison of a 100 MHz 50% duty cycle clock unscrambled and after getting scrambled. The first harmonics show benefit from scrambling, but higher order harmonics are equivalent to the scrambled amplitudes. In fact, a scrambled clock can be worse in terms of impact due to the broadband nature of the signal versus the discrete nature of the unscrambled clock. This is probably more of a concern for RF interference in radio channels than for EMI compliance.

Figure 72. Spectral Comparison of a Clock Scrambled vs. Unscrambled





### 17.4.9 Memory Down

Memory down PCB layout may be challenging to minimize EMI/RFI. Intel recommends the following guidance:

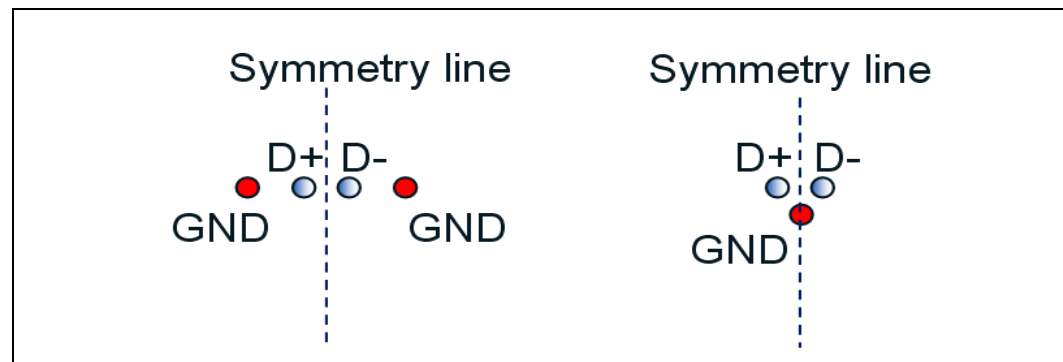
- Place DRAMs closest to CPU.
- Clocks should be at least 3X the trace width away from other traces.
- Solid ground reference to clock, DQ, and DQS.
- Minimize the number of layer transition. There should be at least one ground via nearby each transition.
- No crossing splits (slots and voids).
- No clustered signal vias. They create slots.
- All the traces should be away from the edges of ground planes at least 20X the separation distance between the routing layer and its reference plane.
- IO connector should be at least 1 inch away from clock, DQ, and DQS.

*Note:* Refer to [Chapter 3.0](#) for more detail of topology recommendations.

#### 17.4.9.1 Layer Transition

Layer transition is not avoidable but PCB designers should minimize the number of transitions. Microstrip lines are used for CPU break-out and DRAM fan-in. PCB designer should also minimize the length of microstrip lines. Therefore, one transition happens close to CPU and one happens close to DRAM. In addition, for each transition, there should be at least one ground via nearby to maintain the low impedance of return current path. For differential signal routing, the ground via placement should be symmetry (See [Figure 73](#)).

**Figure 73. Ground Vias Placement**



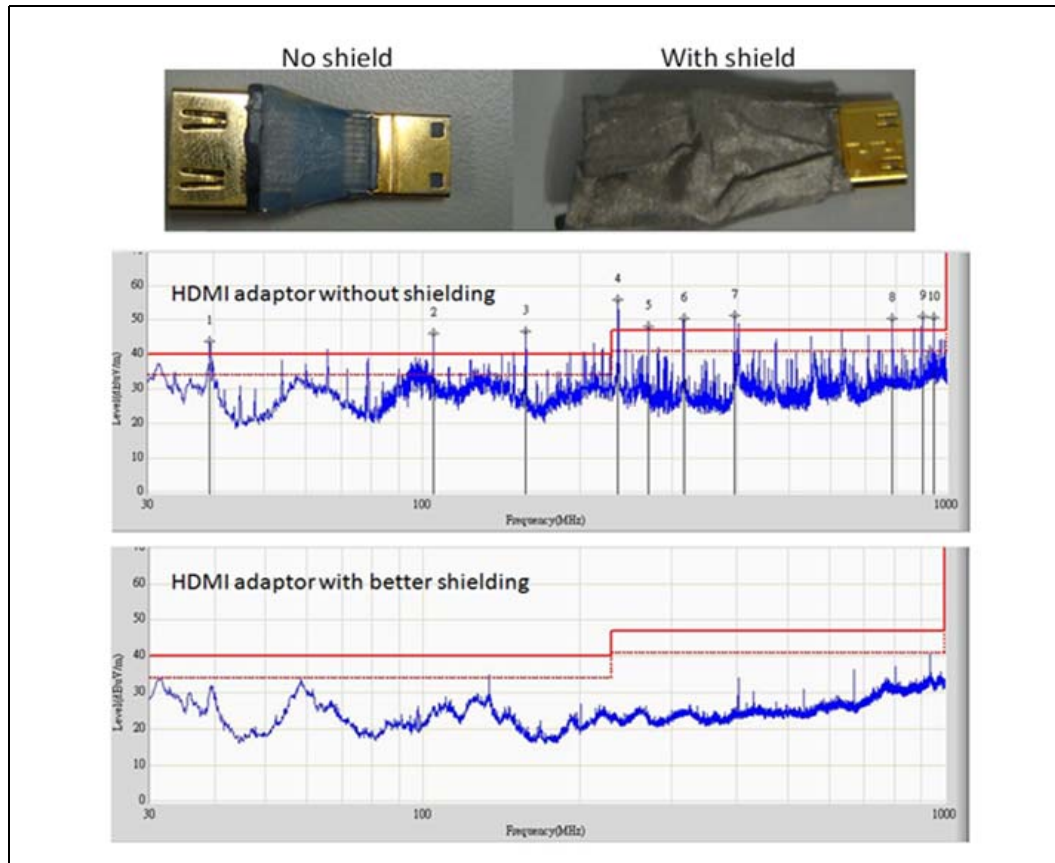
#### 17.4.9.2 Clustered Signal Vias

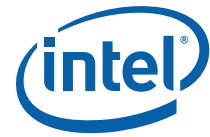
Clustered signal vias should be avoided. There will be many vias for layer transitions. PCB designer should avoid clustered signal vias. Clustered signal vias will create long open slots. Signals such as CLK can cross over these slots. Crossing slot results in high return current impedance and induces higher EMI/RFI radiation. To avoid clustered signal vias, one can insert a ground via every few signal vias.

### 17.4.10 Cable/Adaptor Shielding

During EMI measurement, one may find some EMI violations are from the IOs such as USB and HDMI. Intel recommend check the cable/adaptor shielding quality before implementing a PCB solution, common mode choke for example. [Figure 74](#) shows an example. A mini-HDMI adaptor was used during the EMI measurement. HDMI clock radiated strongly because the adaptor is not well shielded.

**Figure 74. Cable/Adaptor Shielding Impacts EMI Significantly**





## 17.5 Design Checklist Items

This section provides a checklist that should be reviewed during the design process. This checklist has been developed over time and experience to reduce the possibility of unwanted emissions. The checklist is shown below. Not every suggestion is 100% effective; attention to appropriate items can help reduce EMI. The design and layout of the board must be reviewed by the appropriate EMC engineer assigned to the project prior to committing to fabrication.

**Table 56. Component Placement Review Checklist**

ITEM NO.	DESCRIPTION	Y/N
169-1	Clock synthesizers, crystals, oscillators, microprocessor chips and other VLSI packages have been placed in the center of the board, away from board edges, I/O connectors, plane splits and other board mounted connectors to minimize radiation from the board.	
169-2	Components using the same clock have been placed close to each other and the clock source to minimize clock trace lengths.	
169-3	Filter components have been placed adjacent to the pin they are filtering on I/O connectors.	
169-4	For non-differential clocks, provisions have been made for series termination of clock traces at the source to minimize ringing.	

**Table 57. General Routing Review Checklist**

ITEM NO.	DESCRIPTION	Y/N
170-1	Board stack-up designed to insure that all clocks and high-speed (> 1 MHz) traces are routed in layers adjacent to power or ground planes.	
170-2	Power planes have been recessed from the edge of the board.	
170-3	Clock traces have been laid out first and kept as short as possible, consistent with the need for matched clock trace lengths in the clock nets.	
170-4	Clock and High-Speed traces do not change layers and do not cross breaks in power or ground planes. Stitching capacitors must be used in areas where reference breaks are unavoidable.	
170-5	Clock and High-Speed traces have been kept away from board edges and traces leading to connectors (internal or external connections).	
170-6	Clock and High-Speed differential traces have been laid out to minimize length, consistent with the need for matched trace lengths to minimize signal skew.	
170-7	Do not route traces under clock generating circuits or other large high speed devices.	
170-8	Ground pads with the same footprint as the part have been provided on the component side of the board away from oscillators or clocks. These ground pads are tied to the ground plane(s) of the board with multiple vias.	
170-9	Provisions have been made for bonding the board ground system to the chassis at multiple points. The best locations are at connectors and noise sources (clocks, microprocessors, etc.).	
170-10	Provisions have been made for grounding the heat plate or heat sink on the SOC(if applied) to the board ground structure with a maximum spacing between ground points of 375 mils (9.525 mm); $\lambda/10$ .	
170-11	Contiguous memory referencing topology must be maintained.	



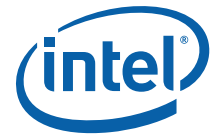
**Table 58. I/O Routing Review Checklist**

ITEM NO.	DESCRIPTION	Y/N
171-1	All I/O connectors have been provided with a low impedance bond to chassis for their shield structure.	
171-2	All non-ground nets routed externally, should have a filter present.	
171-3	I/O connector traces route to ESD protection before any other device.	

**Table 59. Decoupling/Filtering Review Checklist**

ITEM NO.	DESCRIPTION	Y/N
172-1	SMT bypass capacitors are connected directly to power and ground planes with minimum trace length between the part and via.	
172-2	Bypass capacitor values have been selected to insure minimum impedance in the frequency range(s) of interest.	
172-3	Filter capacitors (line to ground) have been provided a low impedance path to chassis as close to the capacitor as possible.	
172-4	All pins on audio connectors have been filtered with both line to ground capacitors and series inductors and/or ferrite beads with the capacitor placed between the inductor/bead and the circuits in the system. These filter elements have been located at the I/O connector.	

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## 18.0 Electrostatic Discharge (ESD)

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### 18.1 Electrostatic Discharge (ESD) General Introduction

#### 18.1.1 Description

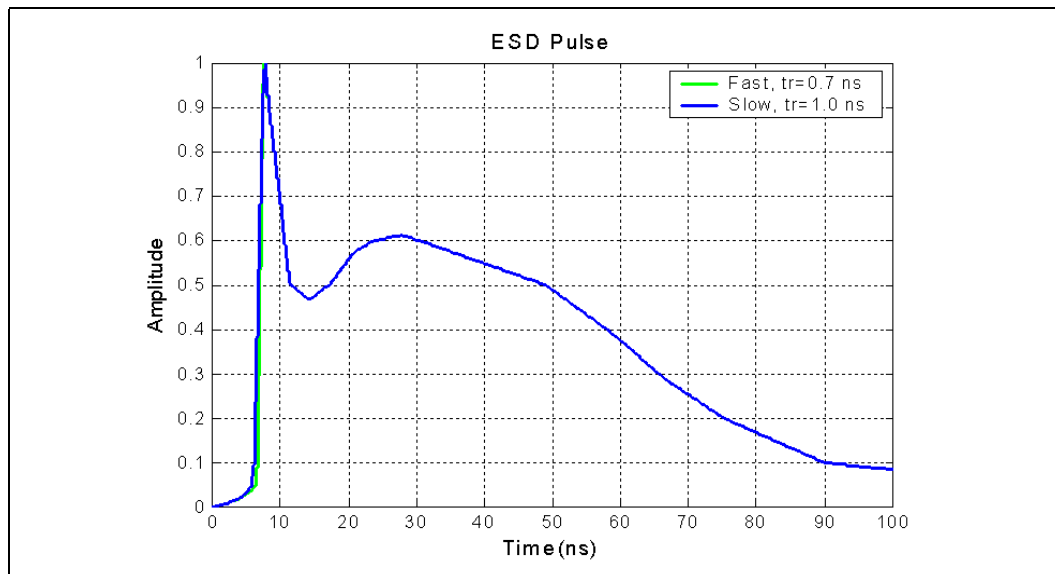
All electronic equipment that is sold into the European Union and mutually recognized countries, must possess the CE mark which designates it has passed a required set of test standards; these test requirements include system testing for ESD protection. The purpose of the ESD test is to demonstrate that a system can withstand static discharges encountered in normal handling and system operation. It is important to emphasize designing for ESD in the early project stages help reduce costly and time consuming debug and design changes late in the development cycle.

Besides standard regulatory requirements for system-level ESD, an emerging threat to component reliability and quality has been the direct and indirect discharge of ESD to the signals and pins of user accessible I/O interfaces; hot-plug. Traditional silicon level ESD protection, meant to handle JEDEC and ESDA procedures, may not be able to respond to the 200ps to 1ns high inrush current of an IEC 61000-4-2 ESD type event.

Depending on the ESD characteristics and level encountered, the failure mode of semiconductors will behave and occur differently. Outside the instantaneous logic error or catastrophic failure, repetitive ESD stress may produce degradation of failures over time and is referred to as latent ESD defects. This occurs when an ESD pulse is not strong enough to destroy a device but alternatively causes undetected degradation. Although the device may suffer this degradation, it may still function within data sheet parameters. A device can be subjected to numerous weak ESD pulses, with each one further degrading a device before it succumbs to a noticeable failure. There is no known practical methodology able to screen for devices with latent defects.

The IEC 61000-4-2 ESD pulse is a transient with a very fast rising edge. The IEC 61000-4-2 specification defines the time domain waveform of the ESD pulse. The risetime of the waveform is between 0.7 ns to 1 ns with a specified peak current of 3.75 A/kV. Additional current waveform requirements are 2 A/kV at 30 ns and 1 A/kV at 60 ns.

Figure 75. IEC 61000-4-2 ESD Waveform



### 18.1.2 Reference Specifications

Title	Location
IEC 61000-4-2	<a href="http://www.iec.ch/">http://www.iec.ch/</a>

## 18.2 ESD Protection

Selection criteria for discreet ESD protection devices must include consideration for the electrical constraints of the interface needing protection. Many discreet semiconductor ESD manufacturers now manufacturer devices for specific low- and high-speed interfaces.

When considering an ESD protection device, it is recommended to select a device with the highest rating against IEC 61000-4-2 air and contact discharge. Typically, the device should be able to withstand a minimum air discharge of ±15 kV and a contact discharge of ±8 kV. Clamping or holding voltage is another parameter that must be selected based on the EOS (Electrical Over Stress) rating of the interface. The lower the clamping voltage rating, the less residual energy will couple to the interface. As signaling BW increases, capacitive loading becomes a serious concern when placing a device on a high-speed interface. The maximum capacitive loading must be considered as it relates to line-to-line and line-to-ground loading. Many devices are being designed to work in the sub-pF range to handle the lower load requirements of high-speed interfaces.

ESD device selection is summarized as:

- 1) Can withstand IEC ESD levels
- 2) Determine maximum clamping voltage before EOS
- 3) Determine maximum capacitive loading allowed

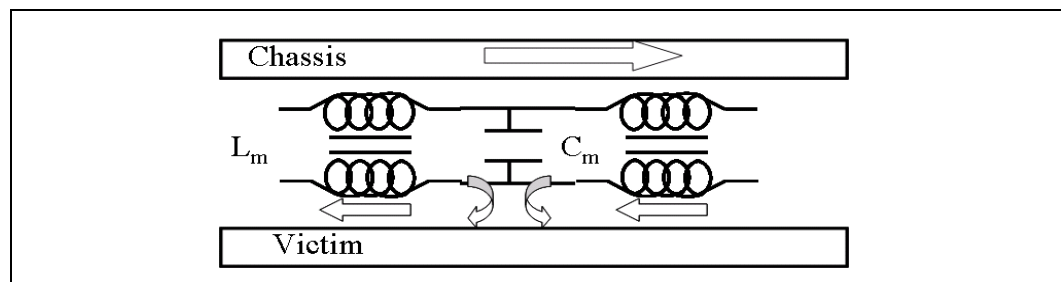
### 18.2.1 ESD Ground-Fill

Reducing sensitivity to Electrostatic Discharge (ESD) to ensure Intel products comply with ESD standards can be a time and cost intensive effort. This section recommends changes to the printed circuit board design that will reduce ESD sensitivity by implementing a low impedance ESD current path to ground, thereby, reducing the coupling to sensitive circuitry.

### 18.2.2 Ground-Fill Background

The premise of system ESD is that the discharge produces a surge through the chassis that induces voltage and current fields within the system. The induced fields produce negative effects to the board and components. The strength of the field coupling is limited by the ESD spectral content, the chassis material thickness and skin depth, size of coupled object, and proximity to the source. The coupling mechanism is a product of mutual inductance and capacitance shown in Figure 76. The energy is high-pass filtered according to the dimensions of the victim as expressed in equations (1).

Figure 76. Mutual L and C ( $L_m$ ,  $C_m$ ) Coupling



The induced voltage can be express as (1):

$$\frac{V_2}{V_1} = \frac{jk \sin \theta}{\sqrt{1 - k^2 \cos \theta + \sin \theta}} \quad \theta = \pi \omega / (2 \omega_0)$$

$\omega_0$  is the  $\frac{1}{4} \lambda$

It is therefore expected that short and thin transmission lines couple very little energy from the chassis discharge, while larger structures like a heatsink, packages, long and thick power traces will couple the bulk of the energy. However, as signal noise margins have shrunk over time, it does not take very much induced noise to disrupt these signals. The area of the chassis that historically has high ESD coupling is the I/O area due to the many penetrations in the chassis necessary to allow the I/O to connect to peripherals. How well these I/O connections are RF bridged, directly impacts the strength of the coupled noise. Along with good I/O shield ground connections, printed circuit board grounding has been heavily depended on to dampen/reduce the coupled energy.

It is the intention to use the naturally occurring coupling to dampen the ESD energy at the most sensitive I/O area through the creation of an electrical large ground fill structure. A metal ground shape will act as a low-pass filter which effectively lowers the Q of coupled circuits. The thickness of the ground fill is required to be greater than the calculated skin depth otherwise currents will form on both sides of the plane. The skin depth can be calculated in the following expression:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

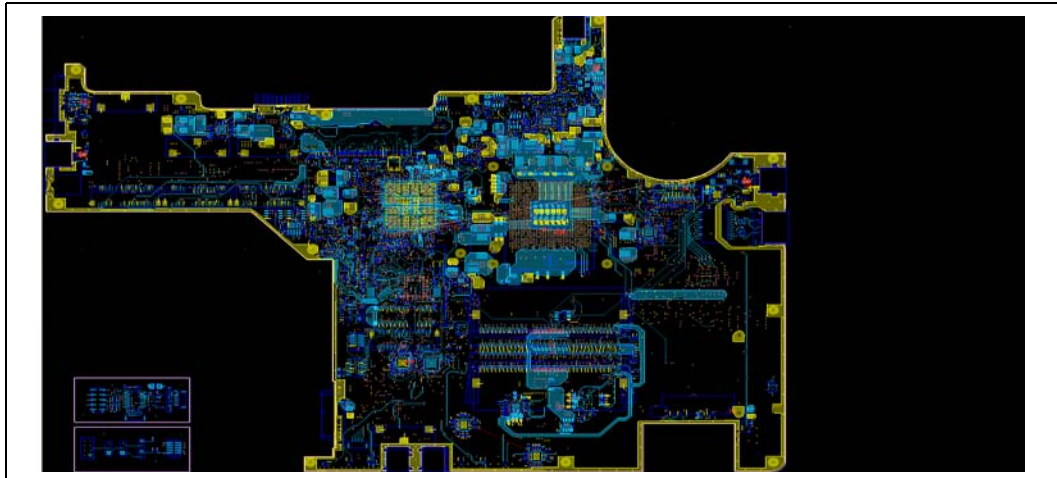
To dampen the ESD energy it will be necessary to create the ground fill large enough to create a strong mutual coupling that has low enough impedance where the energy can be directed to ground. The results would be a drastic reduction in trace coupled noise.

Ground-Fill Procedural Recommendations:

This section describes the step-by-step process used to design an effective ESD ground shape for ESD protection using an example design.

1. Locate the ground shape at the input/output (I.O.) edge of the board on all layers except the ground layer, which should be a solid layer with no spits. Ground shape is highlighted in yellow.

**Figure 77. Ground Shape Along the I/O Edge of the Board**



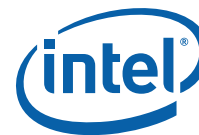
2. The ground shape should be continuous along the edge, outside of any traces. Keep the gap between the ground shape and other shapes or traces at least 20 mils. The minimum shape neck width is 50 mils.
3. Ideally, the ground shape on each layer should connect to at least two mounting holes for noise current to return to the chassis. If the ground shape cannot connect to the mounting holes on every layer, then connections to the mounting holes on at least one layer besides the ground layer should be sufficient, assuming the vertical stitching is ample.
4. The ground shape is useless without proper vertical stitching to the ground layer. Connector holes can be considered stitching vias. Add vias throughout the length of the ground shape, no more than 300 mils apart, close to the board's edge.

### 18.2.3 USB ESD Diode Recommendation

Intel recommends placing ESD protection devices for each USB 2.0 data pair. Selection of USB 2.0 ESD diode should be particularly careful and should be different due to different speeds. Please refer to [Section 18.3.1](#) for USB 2.0 for specific ESD diode recommendation.

### 18.2.4 Series RC Filters

Conventionally ESD protection circuits are composed with ESD diodes or varistors. These non-linear components are activated typically at high voltage (>10 V) to guide injected ESD current from sensitive parts such as ICs. They are very effective when the ESD noise is injected directly into sensitive parts and signal lines. However, when the ESD noise is injected into system ground and/or chassis, the capacitively/inductively



coupled ESD noises show alternative behaviors. These noises typically have lower voltage level (<10 V). They do not activate the aforementioned ESD protection circuits, such as ESD diode, but are still capable of upsetting the system. Therefore, they may have very limited effects against such ESD events.

A series RC filter may be applied sensitive asynchronous nets to enhance the system robustness under such circumstances. This filter can reject high-frequency components in injected ESD noise even when ESD diodes are not activated. The peak voltage and current may be significantly reduced. Due to the low-pass nature of this filter, Intel does not recommend applying this filter to high-speed links. This filter may degrade signal integrity of high speed signaling.

The schematic of this filter is shown in Figure 78. It is a combination of series capacitors and resistors, shunted from the signal line to the ground. Intel recommends the component values of  $R=10\ \Omega$  and  $C=100\ \text{nF}$  for a  $50\text{-}\Omega$  transmission line. The frequency response of this filter is depicted in Figure 79. The first pole can be found around 10 KHz, while the knee point is around 100 MHz. This suppresses high-frequency components of ESD noise with negligible impacts to asynchronous signaling. Intel’s recommendation provides the typical value as a starting point. The components value may be adjusted accordingly to meet pin/signal requirements. It is noted that this filter needs to be placed within 100 mil from the victims (sensitive IC pins) as possible, to ensure the protection effectiveness.

Figure 78. Series RC Filter for ESD Mitigation on Asynchronous Nets

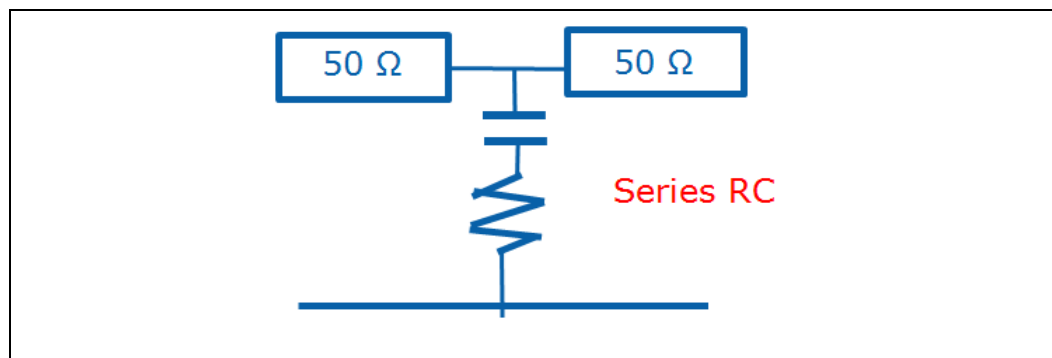
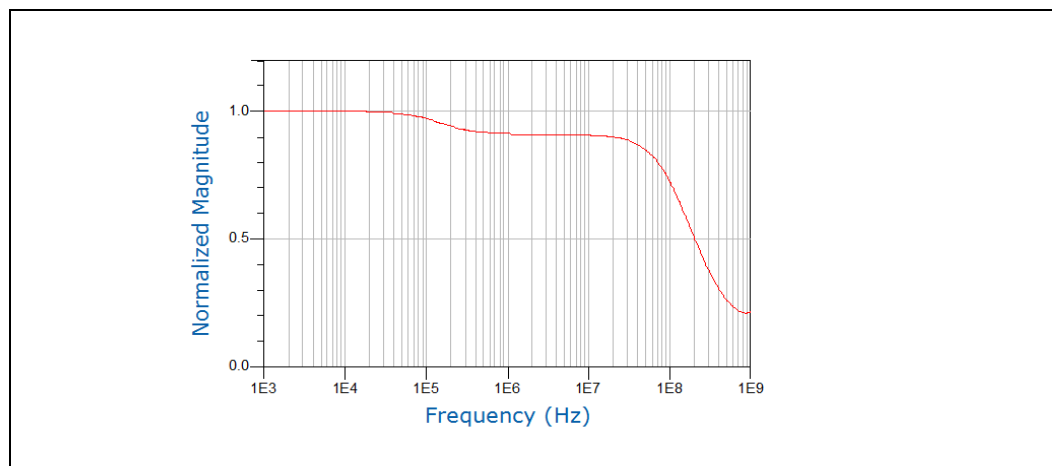


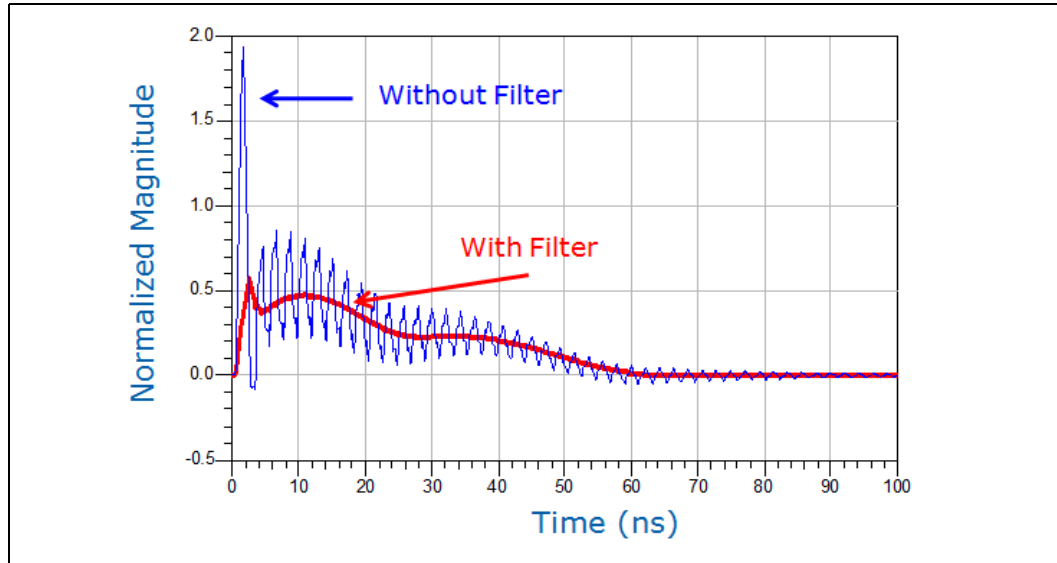
Figure 79. Frequency Response of The Series RC Filter



The effectiveness of this series RC-filter is shown in [Figure 80](#). The magnitude of the sharp peak is effectively reduced by 75% with the series RC filter. The filter has significant impacts on ESD robustness, since this sharp peak contains huge amounts of high-frequency components and is typically the origination of most problematic symptoms in the system. This filter can also suppress the ringing of ESD noise on the transmission line. Typically asynchronous nets are terminated with small capacitance instead of 50-Ω load. This causes impedance mismatch and thus ringing, especially for long traces. Ringing contains high-frequency components and increases local peak-voltage. It may degrade ESD robustness of the system. It has been demonstrated in [Figure 80](#) that the ringing is significantly reduced with the series RC filter.

The impact of the series RC filter to signal integrity is analyzed in [Figure 81](#). The rising and falling edges of the signal remain relatively fast with the presence of the series RC filter. The rising time is about 2.84 ns, measured from 30% to 70% of the signal level. This is sufficiently fast for most of asynchronous nets. One drawback of this filter is that the duration required to reach 99% of the signal level is about 10 μs. However, for operation of typical digital circuits, this has negligible impacts because reaching 99% of the signal level is not required.

**Figure 80. ESD Noise Suppression Using Series RC Filters**



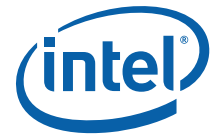
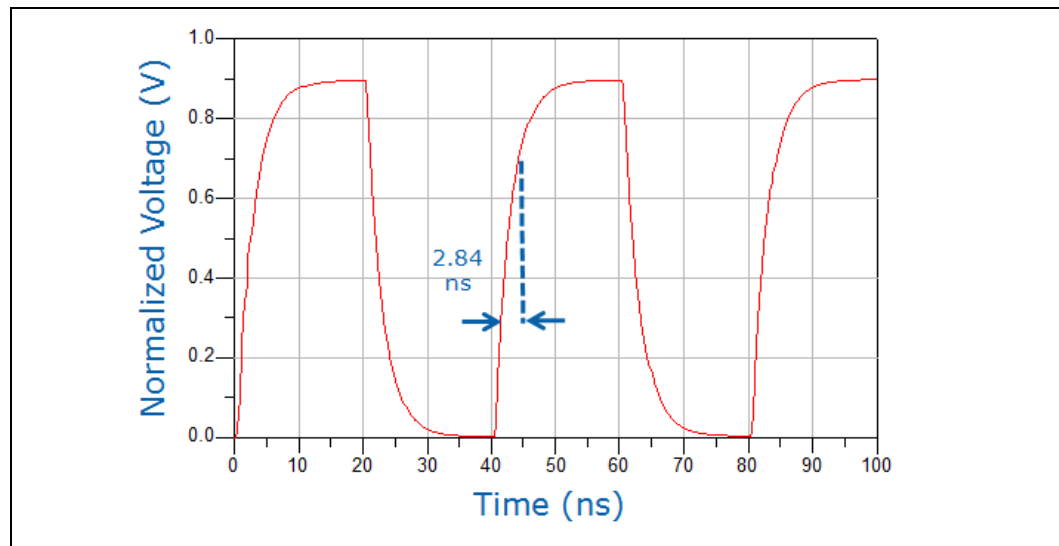


Figure 81. Signal Integrity Analysis With Series RC Filters



### 18.2.5 Sensitive Nets

Understanding the sensitivity of each signal nets to ESD noise may be very helpful for designing and debugging a system for ESD. Certain nets on the platform may have higher sensitivity to ESD noise and have severe impacts to the system. They need extra care in circuit layout. The aforementioned ESD protection circuits may also be populated for such nets to ensure the ESD robustness of the system. It is critical to identify such sensitive nets among hundreds of nets on the platform and narrow down the potential victims to ESD injections. This significantly reduces the required time and cost to solve ESD-related issues.

A test approach to assess net sensitivities on Intel platforms has been developed. In this approach, Transmission line pulser (TLP) is employed to generate a sharp and short pulse to emulate ESD noise. Rising time and pulse width of this pulse are typically less than 5 ns and 50 ns, respectively. It is injected into the system through a TLP probe that directly touch the net under test with ohmic contact, as shown in [Figure 82](#). Unlike commonly-used ESD guns that have large unshielded tip and chassis, the TLP probe is shielded to the very tip and has very limited coupling to proximity nets. This approach focuses on one single net and eliminates the possibilities of stimulating proximity nets. On the contrast, using ESD guns to investigate net sensitivity may be quite misleading. Direct-zapping using ESD guns may stimulate proximity nets and make it difficult to isolate the sensitivity from these proximity nets.

The tested sensitive nets are listed in [Table 60](#). The typical symptoms when these nets are upset are also included. This may be helpful for victim identifying during system debugging.

Figure 82. Circuit Diagram of Direct Injection Method

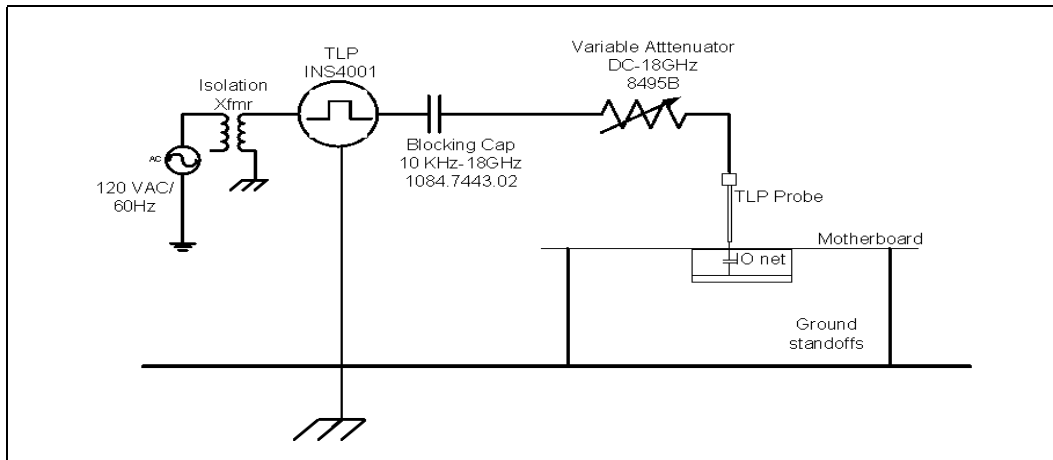


Table 60. Tested Sensitive Nets

Net Name	From	To	Typical Symptoms
Rtc_Rst	Xtal	SOC	Reboot
25M Xtal_Out	Xtal	SOC	Reboot
platform_s5_pwrok	PM	SOC	Reboot
Dram_Rst#	CPU	DDR3	Reboot
platform_s3_pwrok	PM	SOC	Reboot
platform_s0_1p0_pwrok	PM	SOC	Reboot
platform_s0_1P5_pwrok	PM	SOC	Reboot

## 18.3 USB ESD Component Selection Guidelines

### 18.3.1 USB 2.0 ESD Protection

USB components and ICs are heavily subjected to frequent human contact due to its hot plugging usage model nature where there is a high frequency of insertion and removal of various USB devices from the USB ports. As a result, USB ports are easily exposed to ESD strikes from the human body that can destroy both the USB host and devices on the platform. ESD discharges from human contact could easily go up to ~35kV under extreme cases; therefore USB ports need to be protected.

There are currently a vast variety of ESD protection devices that are readily available in the market such as Metal Oxide Varistors (MOVs), Zener Diode, Transient Voltage Suppressor (TVS), Polymer devices and dual rail clamp diodes. Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of high-speed data. With 480Mbps of data rate, USB 2.0 is very sensitive to parasitic capacitance in its signal path. A tiny amount of parasitic capacitance in the pF range could distort USB signal, possibly causing the USB signal to fail and devices not working properly. In order to meet the stringent requirement on device capacitive load, the Dual Rail Clamp Diodes, which have the lowest capacitance among the ESD protection devices, is found to be the best option for USB 2.0 ESD protection. Figure 83 shows the circuitry of a dual rail clamp diode.



Figure 83. USB 2.0 ESD Protection Devices

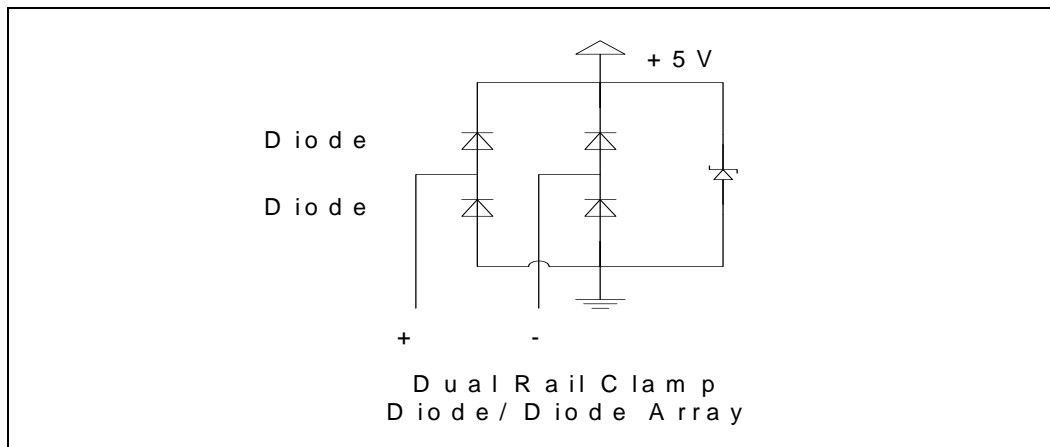
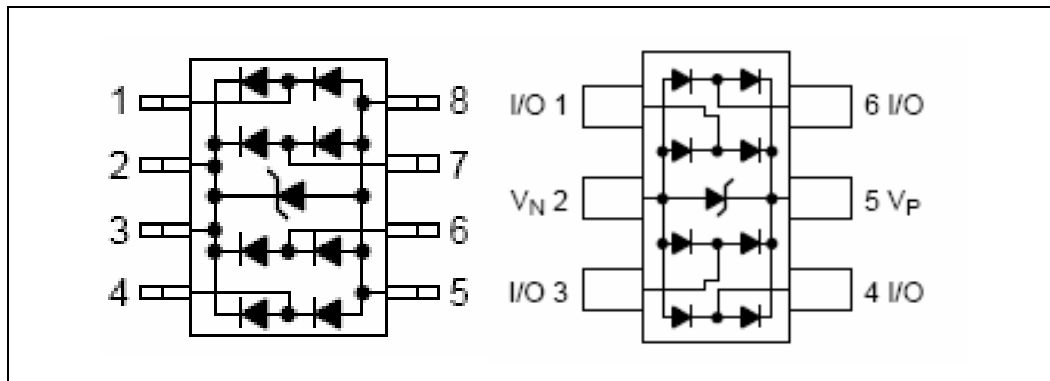
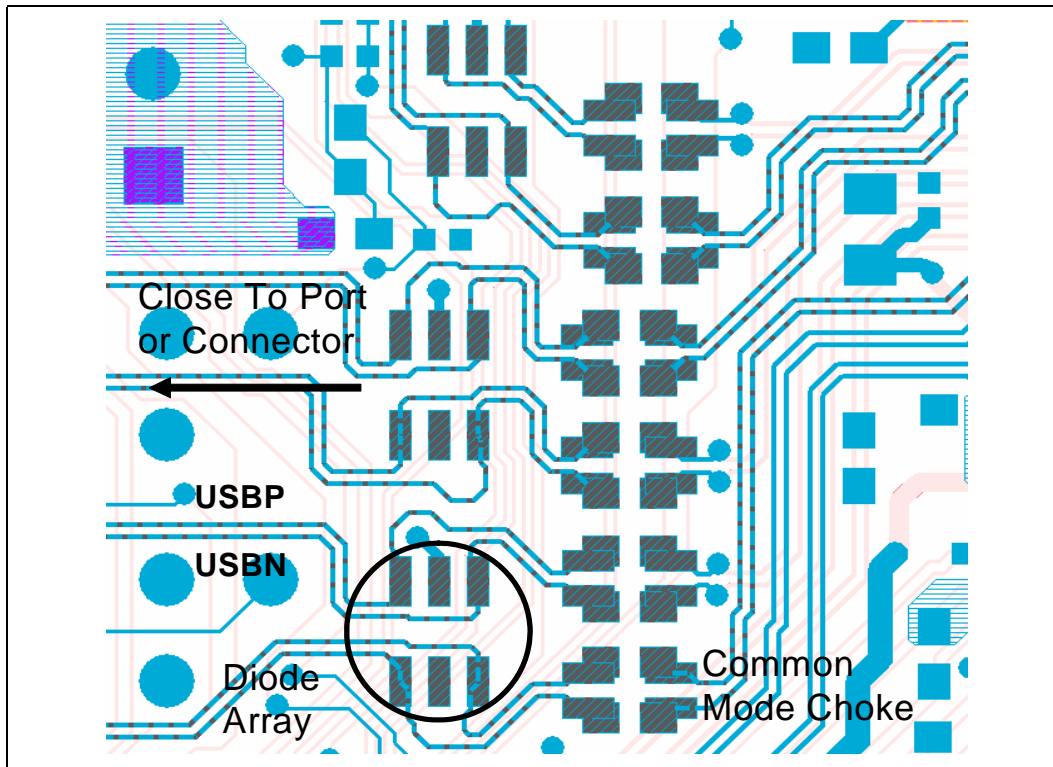


Figure 84. Typical Integrated Diode Array Package



Proper placement of any ESD protection device is on the data lines between the common mode choke and the USB connector data pins as shown in [Figure 85](#). The ESD protection devices should be placed as close to the USB connector as possible so that when ESD strikes occur, the discharges can be quickly absorbed or diverted to the ground/power plane before it is coupled to another signal path nearby. Proper placement of ESD protection device can improve the effectiveness of protecting the system against ESD strikes. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, the Dual Rail Clamp Diode ESD protection device is needed.

Figure 85. Layout Example of USB 2.0 with ESD Diode Array



Using ESD protection devices with higher parasitic capacitance would impact the USB2.0 signal quality and thus limit the routing solution space of USB.

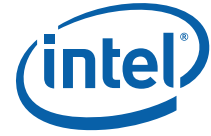
*Note:* Further ESD information is detailed in the high speed USB Platform Design Guides available at [www.usb.org/developers/docs.html](http://www.usb.org/developers/docs.html)

Recommended characteristics of an ideal ESD Protection Diode for USB2.0 are:

- Able to withstand at least 8kV of ESD strikes, complying to IEC 61000-4-2 standard.
- Low Capacitance, <2pF to minimize signal distortion at high speed data rate.
- Fast response time to protect from the fast rise time of ESD surge pulses.
- Low Leakage Current to minimize static power consumption.
- Integrated and reduced package dimension for better real estate and smaller parasitic package effect.
- High reliability -Robustness to drive and absorb repetitive ESD conditions without damage.

### 18.3.2 USB 2.0 ESD Protection Diode Vendors

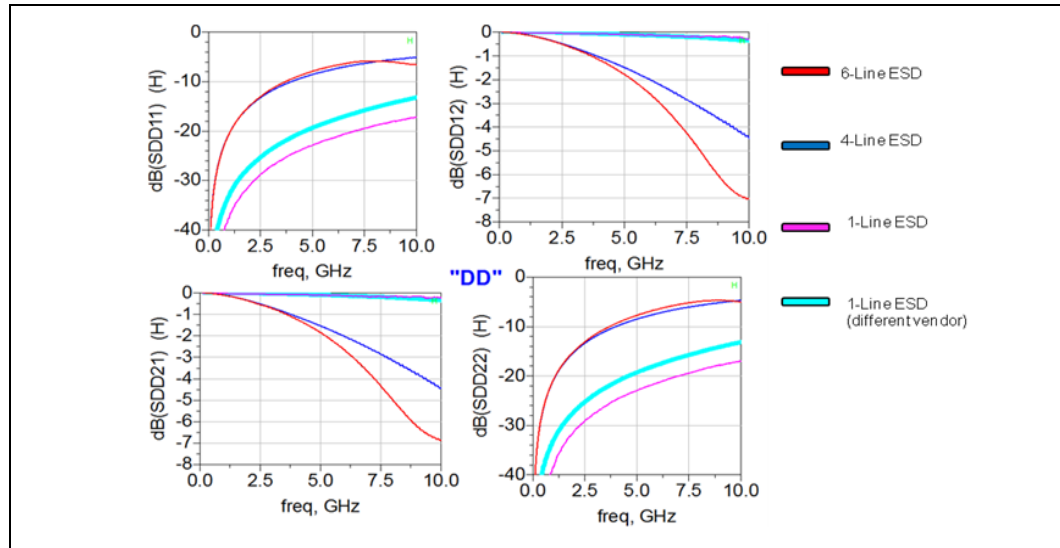
ESD suppression is always recommended by Intel. However Intel does not recommend a specific part/device or circuit for ESD suppression because each solution is board/chassis/usage model specific. The following vendors manufacture ESD protection Diode for USB2.0 which conform to the IEC 61000-4-2 standard. Please contact ESD protection device vendors for more specific details on devices availability, packaging option, how to place and optimize ESD, and datasheet.



- CalMicro: <http://www.calmicro.com>
- ONSEMI: <http://www.onsemi.com>
- Philips: <http://www.philips.com>
- Protek Devices: <http://www.protekdevices.com>
- SEMTECH: <http://www.semtech.com>
- STMicro: <http://www.st.com>

*Note:* This is not an extensive list. There may be others. Please check with your preferred vendor to determine if a compatible device is available.

**Figure 86. Differential S-parameters from Ceramic 1-line, Si 4-line and Si 6-line ESD Protection Devices.**





## 18.4 Design Checklist Items

This section provides a checklist that should be reviewed during the design process. This checklist has been developed over time and experience to reduce the possibility of unwanted ESD risk. The checklist is shown below. Not every suggestion is 100% effective; attention to appropriate items can help reduce ESD risk. The design and layout of the board must be reviewed by the appropriate ESD engineer assigned to the project prior to committing to fabrication.

**Table 61. ESD Checklist**

ITEM NO.	DESCRIPTION	Y/N
173-1	All hot-plug interfaces, should have ESD protection present.	
173-2	Implement a ground shape continuous along the board edge, outside of any traces. Keep the gap between the ground shape and other shapes or traces at least 20 mils. The minimum shape neck width is 50 mils. The minimum fill area should be 20% of the connector footprint under each connector.	
173-3	Add stitching vias throughout the length of the ground shape, no more than 300 mils apart, close to the board's edge (connector holes can be considered stitching vias).	

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## 19.0 Platform Debug and Test Hooks

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### 19.1 Platform Debug and Test Hooks General Introduction

#### 19.1.1 Description

Intel is committed to reducing debug time and cost for OEMs and system integrators. Many debug features and test hooks can be designed into the platform to help reduce these factors. The following section provides an overview of the Intel® Quark SoC X1000 debug and test hooks.

### 19.2 Platform Debug Port

**JTAG Probe** - The Intel® Quark SoC X1000 uses this option to impact the nature of Intel® Quark SoC X1000-based designs where there is no room to support a 60-pin Merged XDP connector.

- Keep Out Zone (KOZ) is required around processor.
- JTAG routing on the platform is required.
- Provides access to SoC JTAG signals, processor configuration signals and others.
- Provides access to SoC test interface signals. A Logic Analyzer (LA) connector footprint is not required.

#### 19.2.1 Signal Routing Guidelines

JTAG signal routing topology requirements are different from previous designs. Guidelines for routing the JTAG pins can be found in the Intel® Quark SoC X1000 *Platform - Debug Port Design Guide*.

### 19.3 JTAG Boundary Scan

The SoC includes a JTAG (TAP) port compatible with the *IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1 Specification*. The TAP controller is accessed serially through the five pins TCK, TMS, TDI, TDO, and TRST\_B#. Additionally routing the PRDY\_B and PREQ\_B to the header would be advantageous from a debug perspective.

TMS, TDI and TDO operate synchronously with TCK which is independent of all other clock within the SOC. TRST\_B#, per the specification, is an optional signal. This 5-pin interface can be used for test and debug purposes. System board interconnects can be DC tested using the boundary scan logic in pads.

#### 19.3.1 Terminating Unused JTAG Signals

When unused, all JTAG pins should be pulled according to the following table.



Table 62. JTAG PullUp / PullDown Requirements

Pin	Direction	PullUp/PullDowns
TCK	Input	Internal 20K Pull Down
TDI	Input	Internal 20K Pull Up
TMS	Input	Internal 20K Pull Up
TRST_B	Input	Internal 20K Pull Up
TDO	Output	Internal 1K Pull Up
PREQ_B	Input	Internal 20K Pull Up
PRDY_B	Output	None

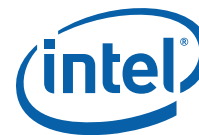
## 19.4 Additional Debug Support Guidelines

### 19.4.1 Test Points Requirements

Intel recommends users at least provide through-hole vias in a location that is probe accessible (avoid location that is blocked by thermal solutions or other mechanical components) and/or pull-up/pull-down resistors, for all the test points so that Intel would be able to access them when debug by Intel is required.

These test points are for debug and validation purposes, when adding test points effort must ensure they are not at the detriment of signal integrity.

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## 20.0 Design for Testability (DFT)

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### 20.1 DFT General Introduction

#### 20.1.1 Description

This section provides guidelines for implementing Design for Testability (DFT) on this platform for supporting customer to define their DFT into their product in order to maximize test coverage in manufacturing tests.

All interfaces will support a minimum of one test bead per signal and a maximum of two test beads per signal. When implementing DFT, it is recommended to use existing vias, pads or pins wherever possible. If existing vias or pads can not be used, they may be added but the total number of vias specified for each interface can not be exceeded.

#### 20.1.2 Reference Documents

Title	Location
<i>VREG Controller's data sheet</i>	TBD
<i>Intel® Quark SoC X1000 Datasheet</i>	<a href="https://communities.intel.com/community/makers/documentation/quarkdocuments">https://communities.intel.com/community/makers/documentation/quarkdocuments</a>

### 20.2 DFT Configuration, Connectivity, Block Diagram

DFT probe points can be placed anywhere on the trace. It is preferred to place test beads directly on the trace or vias. However, if beads can not be placed directly on the trace, the stub to the bead should be less than 50 mils (1.27 mm), shown in [Figure 87](#). Test beads for differential signals should be matched on the differential pair within ±5 mils. If required, it is ok to break the differential pair spacing requirements for a short route in order to place both test beads in a matched location.

Example is shown in [Figure 88](#). Also, it is recommended to place test beads at the end or beginning of a trace in order to avoid signal reflection/refraction.

Figure 87. Example of Test Bead on a Stub (Not Preferred)

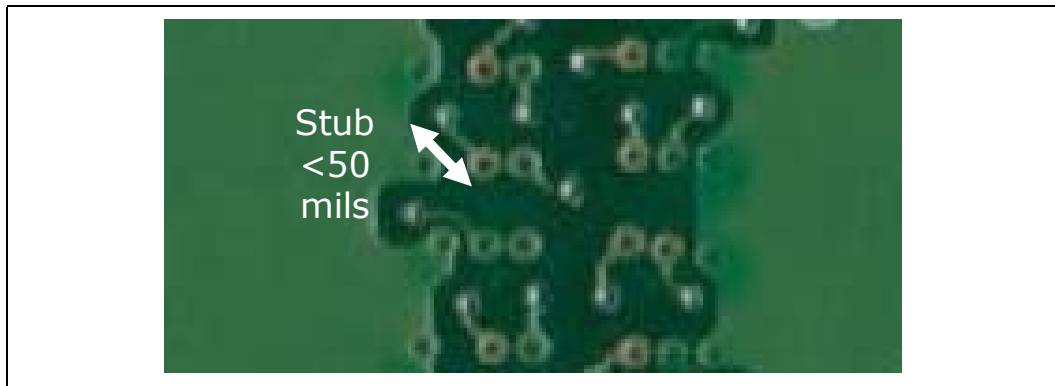


Figure 88. Example of Differential Test Bead with Matched Placement

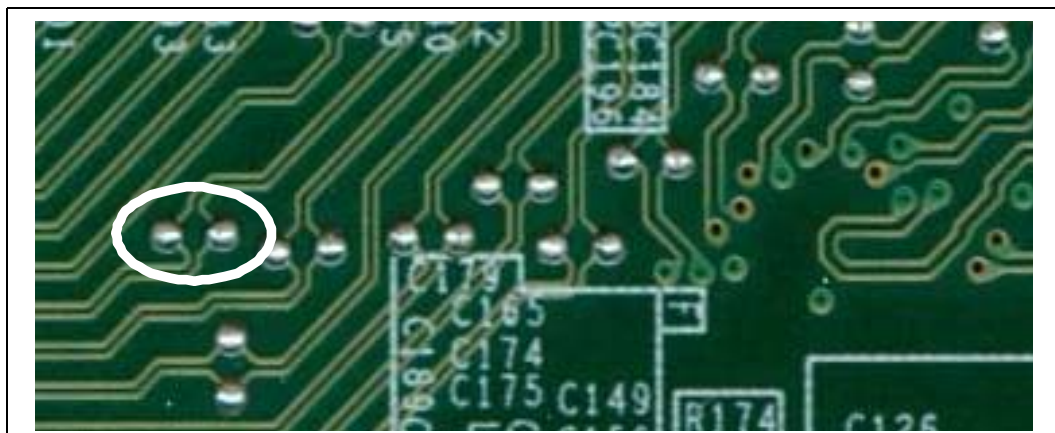
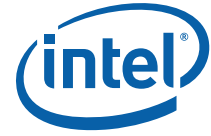


Table 63. Bead Parameters (Sheet 1 of 2)

Parameter	Units	Recommendation	
		Beads formed over solder-mask-openings	Beads placed on existing vias
Test Bead Width	mils	4-7	NA
Test Bead Length	mils	20	NA
Test Bead Diameter	mils	NA	20
Test Bead Height (before being hit by probe)	mils	7-8	5-6
Test Bead Height (after being hit by probe)	mils	5	5
Typical Bead-to-Bead Pitch requirement <sup>1</sup>	mils	50	50



**Table 63. Bead Parameters (Sheet 2 of 2)**

Parameter	Units	Recommendation	
		Beads formed over solder-mask-openings	Beads placed on existing vias
Typical Bead-to-Component Pitch requirement <sup>1</sup>	mils	25	25
Typical flying probe diameter	mils	36	36

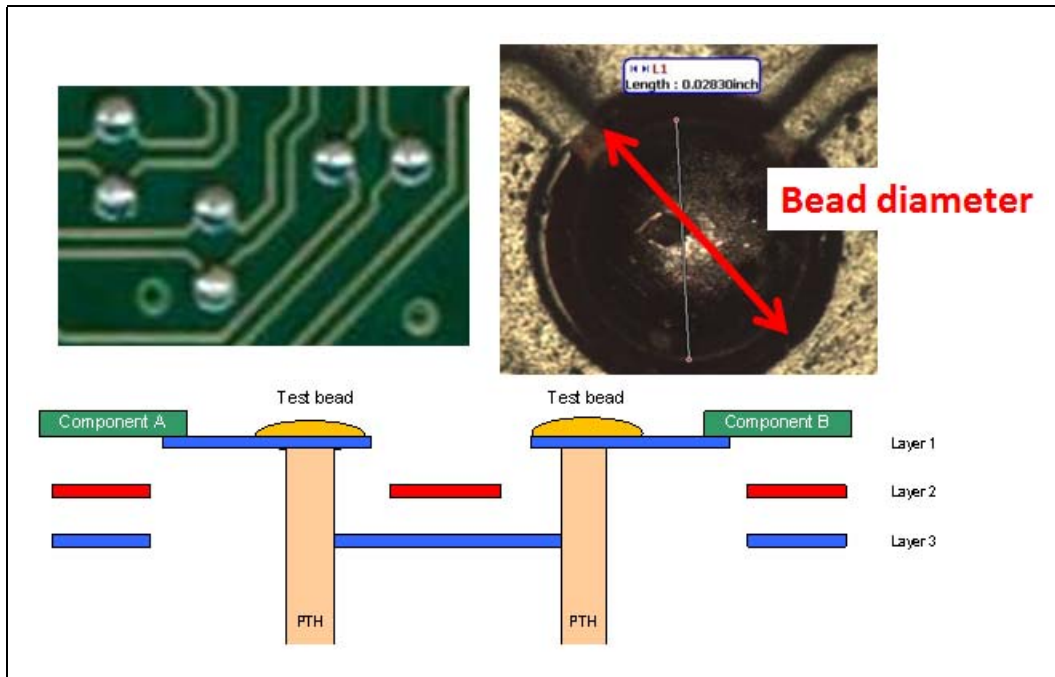
**Notes:**

1. Bead-to-Bead pitch and bead-to-component requirements are based on the bed-of-nails or probe capabilities. Customers should work with their specific vendors to determine what the minimum placement requirements are.
2. This is the actual diameter of the probe being used to take measurements. Customers should work with their specific vendors to determine what their minimum flying probe diameter is.

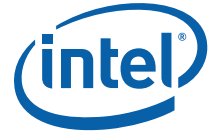
**Figure 89. Bead Formed Over Solder-Mask Opening**



Figure 90. Bead Placed on Existing Via



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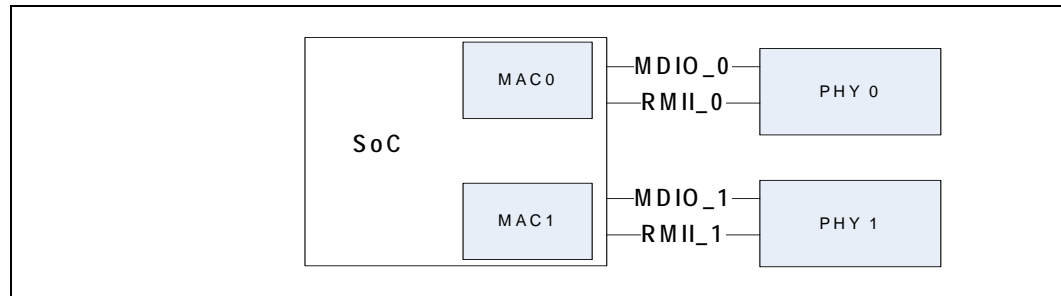


## 21.0 LAN Design Considerations and Guidelines

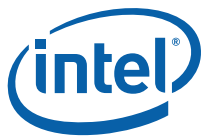
The Intel® Quark SoC X1000 incorporates an integrated 10/100 Mbps MAC controller that can be used with an external PHY shown in [Figure 91](#). Its bus master capabilities enable the component to process high-level commands and perform multiple operations, which lowers processor use by off loading communication tasks from the processor.

The SoC, which hereinafter refers to the integrated MAC within the SoC, supports an MDIO interface for manageability. The integrated MAC supports multi-speed operation (10/100 Mbps). The integrated MAC also operates in full-duplex at all supported speeds or half-duplex at 10/100 Mbps as well as adhering to the IEEE 802.3x Flow Control Specification.

**Figure 91. SOC/PHY Interface Connections**



*Note:* The following sections are based on the TI DP83848I Port 10/100 Mb/s Ethernet PHY.

**Table 64. MDIO Data Signals on the Intel® Quark SoC X1000**

Group	PHY Signal Name	SOC Signal Name	Description
MAC_0 Data	MDIO	MAC0_MDIO	MDIO data
MAC_1 Data	MDIO	MAC1_MDIO	MDIO data

**Table 65. RMII Signals**

Group	PHY Signal Name	SOC Signal Name	Description
MAC_0 Data	TXD_0 TXD_1	MAC0_RXDATA[1:0]	SoC receive data
MAC_0 Data	RXD_0 RXD_1	MAC0_TXDATA[1:0]	SoC transmit data
MAC_1 Data	TXD_0 TXD_1	MAC1_RXDATA[1:0]	SoC receive data
MAC_1 Data	RXD_0 RXD_1	MAC1_TXDATA[1:0]	SoC transmit data
MAC_0 Ctrl	TX_EN	MAC0_TXEN	SoC MAC0 transmit enable
MAC_0 Ctrl	RX_DV	MAC0_RXDV	SoC MAC0 Receive data valid
MAC_1 Ctrl	TX_EN	MAC1_TXEN	SoC MAC1 transmit enable
MAC_1 Ctrl	RX_DV	MAC1_RXDV	SoC MAC1 Receive data valid

**Table 66. Clock and Reset Signals**

Group	PHY Signal Name	SOC Signal Name	Description
Clock	MDC	MAC0_MDC	MAC0 management data clock
Clock	MDC	MAC1_MDC	MAC1 management data clock
Clock	X1	RMII_REF_CLK	RMII PHY reference clock

## 21.1 PHY Overview

The PHY is a single port compact component designed for 10/100Mbps operation. The PHY provides a standard IEEE 802.3u Ethernet interface for 10BASE-TX, and 10BASE-T applications.

### 21.1.1 PHY Interconnects

The main interfaces for either PHY are MDIO and RMII on the host side and Media Dependent Interface (MDI) on the link side. Transmit traffic is received from the SoC as RMII packets on the host interconnect and transmitted as Ethernet packets on the MDI link. Receive traffic arrives as Ethernet packets on the MDI link and transferred to the SoC through the RMII interconnect.



## 21.1.2 RMI I Interface

### 21.1.2.1 RMI I Interface Signals

The signals used to connect between the SoC and the PHY in this mode are:

- Two receive data bits running at 10/100 Mb/s for Rx.
- Two transmit data bits running at 10/100 Mb/s for Tx.
- 50 MHz reference clock input to the PHY is generated by the SOC.
- Transmit enable indicator from SOC to PHY.
- Receive data valid from PHY to SOC with receive data.

The PHY transmit/receive pins are output/input signals and are connected to the SOC as listed in [Table 64](#) through [Table 66](#).

### 21.1.2.2 RMI I Reference Clock

The RMI I Interface uses a 50 MHz reference clock, denoted RMI I\_REF\_CLK. This signal is generated from the SoC and routed to the PHY port and in to the MAC port reference clock.

The frequency tolerance for the RMI I reference clock is  $\pm 50$  ppm.

## 21.1.3 MDIO Interface

MDIO is a low speed (2.5 MHz) serial bus used to connect various components in a system. MDIO is used as an interface to pass management and configuration messages between the PHY and the SOC

The MDIO uses two primary signals: MDC and MDIO, to communicate. MDC is pulled up with a 4.7k $\Omega$  resistor and MDIO is pulled up with a 1.5k $\Omega$  resistor.

### 21.1.3.1 MDIO Connectivity

[Table 64](#) through [Table 66](#) list the relationship between PHY MDIO pins to the SoC LAN MDIO pins.

*Note:* The MDIO signals (MDIO and MDC) cannot be connected to any other devices other than the integrated MAC. Connect the MDIO and MDC pins to the integrated MAC0/1 MDIO and MDC pins, respectively.

## 21.2 Platform LAN Design Guidelines

These sections provide recommendations for selecting components and connecting special pins. For Ethernet designs, the main elements are Intel® Quark SoC X1000, PHYs, a magnetics modules, RJ-45 connectors and a clock source.

### 21.2.1 General Design Considerations for PHYs

Sound engineering practices must be followed with respect to unused inputs by terminating them with pull-up or pull-down resistors, unless otherwise specified in a datasheet, design guide or reference schematic. Pull-up or pull-down resistors must not be attached to any balls identified as “No Connect.” These devices might have special test modes that could be entered unintentionally.



### 21.2.1.1 Clock Source

All designs require a 50 MHz clock source. The PHY uses the 50 MHz source to generate internal clocks for both the PHY circuits and the RMII interface. SoC generates this 50MHz reference clock internally and is passed out of the SoC for routing to the PHY and back to the MAC reference clock port. This methodology manages the clock skew externally rather than resolving it internally. There are three steps to crystal qualification:

1. Verify that the vendor’s published specifications in the component datasheet meet the required conditions for frequency, frequency tolerance, temperature, oscillation mode and load capacitance as specified in the respective datasheet.
2. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems.
3. Independently measure the component’s electrical parameters in real systems. Measure frequency at a test output to avoid test probe loading effects at the PHY. Check that the measured behavior is consistent from sample to sample and that measurements meet the published specifications. For crystals, it is also important to examine startup behavior while varying system voltage and temperature.

### 21.2.1.2 Magnetics Module

The magnetics module has a critical effect on overall IEEE and emissions conformance. The device should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Carefully qualifying new magnetics modules prevents problems that might arise because of interactions with other components or the printed circuit board itself.

The steps involved in magnetics module qualification are similar to those for crystal qualification:

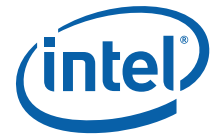
1. Verify that the vendor’s published specifications in the component datasheet meet or exceed the required IEEE specifications.
2. Independently measure the component’s electrical parameters on the test bench, checking samples from multiple lots. Check that the measured behavior is consistent from sample to sample and that measurements meet the published specifications.
3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems. Vary temperature and voltage while performing system level tests.

### 21.2.1.3 Criteria for Integrated Magnetics Electrical Qualification

The following table gives the criteria used to qualify integrated magnetics.

Table 67. Integrated Magnetics Recommended Qualification Criteria (Sheet 1 of 2)

Open Circuit Inductance (OCL)	w/8 mA DC bias; at 25C	400 uH Min
	w/8 mA DC bias; at 0C to 70C	350 uH Min
Insertion Loss	100 kHz through 999 kHz	1 dB Max
	1.0 MHz through 60.0 MHz	0.6 dB Max
	60.1 MHz through 80.0 MHz	0.8 dB Max
	80.1 MHz through 100.0 MHz	1.0 dB Max
	100.1 MHz through 125.0 MHz	2.4 dB Max

**Table 67. Integrated Magnetics Recommended Qualification Criteria (Sheet 2 of 2)**

<b>Return Loss</b>	1.0 MHz through 40.0 MHz 40.1 MHz through 100.0 MHz When reference impedance is 85 Ohms, 100 Ohms, and 115 Ohms. Note that R.L. values may vary with MDI trace lengths. The LAN magnetics may need to be measured in the platform where it will be used.	18.0 dB Min $12 - 20 * \text{LOG}(\text{Freq in MHz} / 80)$ dB Min
<b>Crosstalk Isolation Discrete Modules</b>	1.0 MHz through 29.9 MHz 30.0 MHz through 250.0 MHz 250.1 MHz through 375.0 MHz	$-50.3 + (8.8 * (\text{Freq in MHz} / 30))$ dB Max $-(26 - (16.8 * (\text{LOG}(\text{Freq in MHz} / 250 \text{ MHz}))))$ dB Max -26.0 dB Max
<b>Crosstalk Isolation Integrated Modules (Proposed)</b>	1.0 MHz through 10 MHz 10.0 MHz through 100.0 MHz 100 MHz through 375.0 MHz	$-50.8 + (8.8 * (\text{Freq in MHz} / 10))$ dB Max $-(26 - (16.8 * (\text{LOG}(\text{Freq in MHz} / 100 \text{ MHz}))))$ dB Max -26.0 dB Max
<b>Diff to CMR</b>	1 MHz through 29.9 MHz 30.0 MHz through 500 MHz	$-40.2 + (5.3 * ((\text{Freq in MHz} / 30)))$ dB Max $-(22 - (14 * (\text{LOG}((\text{Freq in MHz} / 250))))$ dB Max
<b>CM to CMR</b>	1 MHz through 270 MHz 270.1 MHz through 300 MHz 300.1 MHz through 500 MHz	$-57 + (38 * ((\text{Freq in MHz} / 270)))$ dB Max $-17 - 2 * ((300 - (\text{Freq in MHz}) / 30)$ dB Max -17 dB Max
<b>Hi-Voltage Isolation</b>	1500 Vrms at 50 or 60 Hz for 60 sec. or: 2250 Vdc for 60 seconds	Minimum

### 21.2.2 NVM Configuration for PHY Implementations

The LAN configuration is programmed via the legacy SPI Flash, which is connected to the SoC. Several words of the non-volatile memory are accessed automatically by the SoC after reset to provide pre-boot configuration data before it is accessed by host software. The NVM space is used by software for storing the MAC address, serial numbers, and additional information. More details may be obtained from the Datasheet.

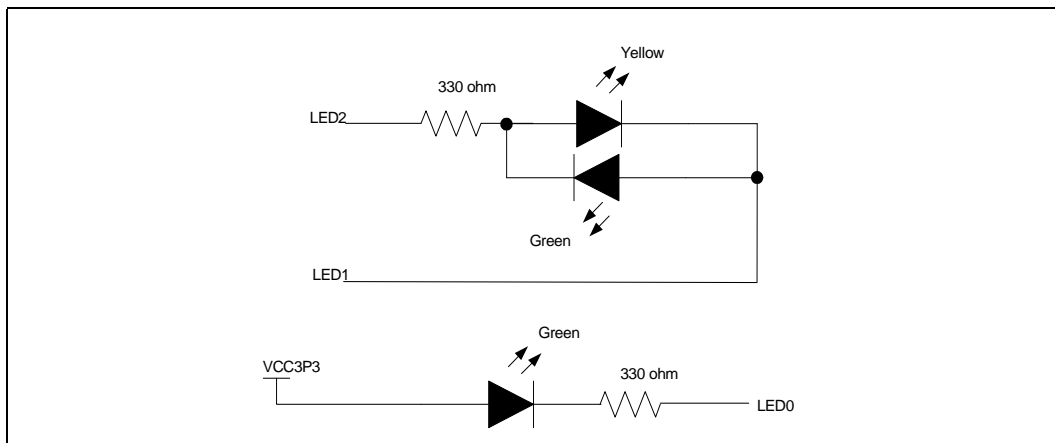
Intel has a software utility called EUpdate that is used to program the SPI Flash images in development or production line environments. A copy of this program can be obtained through your Intel representative.

### 21.2.3 LED Example

Where the PHY has LED outputs that can be configured via the NVM. An example hardware configuration is shown in [Figure 92](#).

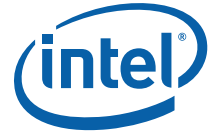
Refer to the Datasheet for details regarding the programming of the LED's and the various modes.

Figure 92. LED Hardware Configuration



### 21.2.3.1 RBIAS

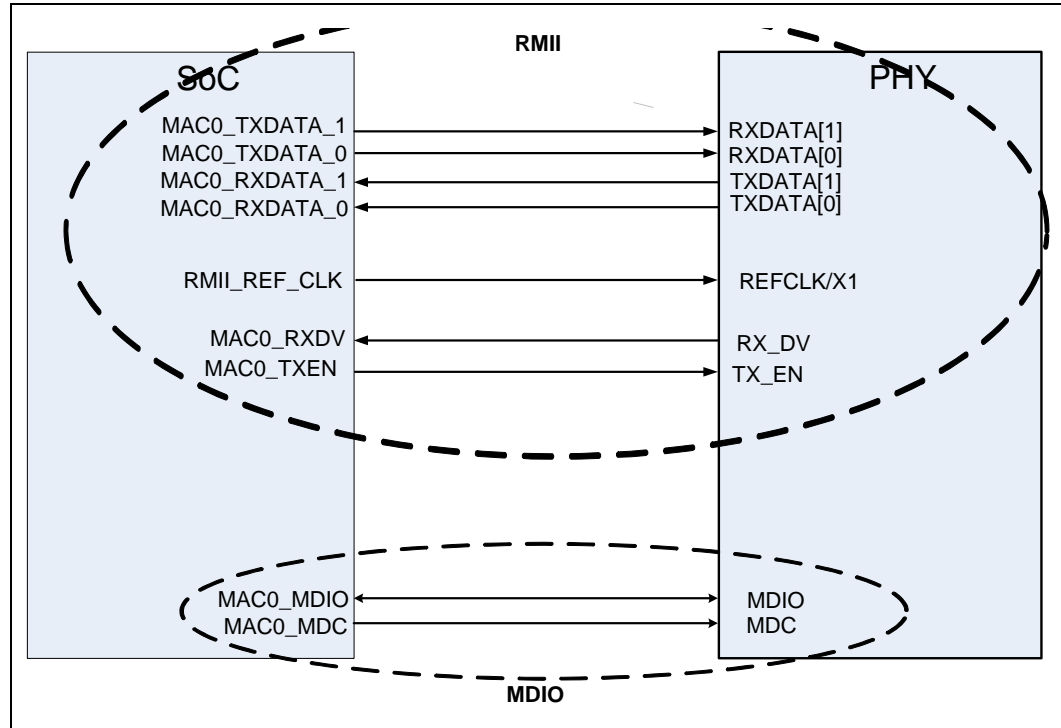
RBIAS requires external resistor connection to bias the internal analog section of the device. The input is sensitive to the resistor value. Resistors of 1% tolerance must be used. Connect RBIAS through a 4.87 kΩ 1% pull-down resistor to ground and then place it no more than one half inch (0.5") away from the PHY.



### 21.3 Intel® Quark SoC X1000 – MDIO/RMII LOM Design Guidelines

This section contains guidelines on how to implement a SoC/PHY single solution on a system motherboard. It should not be treated as a specification, and the system designer must ensure through simulations or other techniques that the system meets the specified timings. The following are guidelines for both SoC MDIO and RMII interfaces.

Figure 93. Single PHY Solution Interconnect





## 21.4 General Layout Guidelines

PHY interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of their respective interface specifications. The following are some general guidelines that should be followed in designing a LAN solution. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk.

## 21.5 Layout Considerations

Critical signal traces should be kept as short as possible to decrease the likelihood of effects by high frequency noise of other signals, including noise carried on power and ground planes. This can also reduce capacitive loading.

Since the transmission line medium extends onto the printed circuit board, layout and routing of differential signal pairs must be done carefully.

For the PHY, system level tests should be performed at two speeds.

## 21.6 Guidelines for Component Placement

Component placement can affect signal quality, emissions, and component operating temperature. Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet applicable government test specifications. In this case, place the PHY more than one inch from the edge of the board.
- Simplify the task of routing traces. To some extent, component orientation affects the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

### 21.6.1 PHY Placement Recommendations

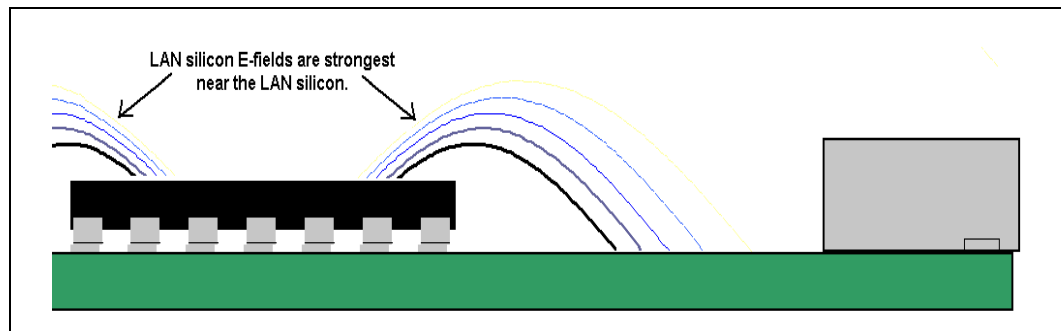
Minimizing the amount of space needed for the PHY is important because other interfaces compete for physical space on a motherboard near the connector. The PHY circuits need to be as close as possible to the connector.

The following figure illustrates some basic placement distance guidelines. To simplify the diagram, it shows only two differential pairs, but the layout can be generalized for a 100MbE system with four analog pairs. The ideal placement for the PHY (LAN silicon) is approximately one inch behind the magnetics module.

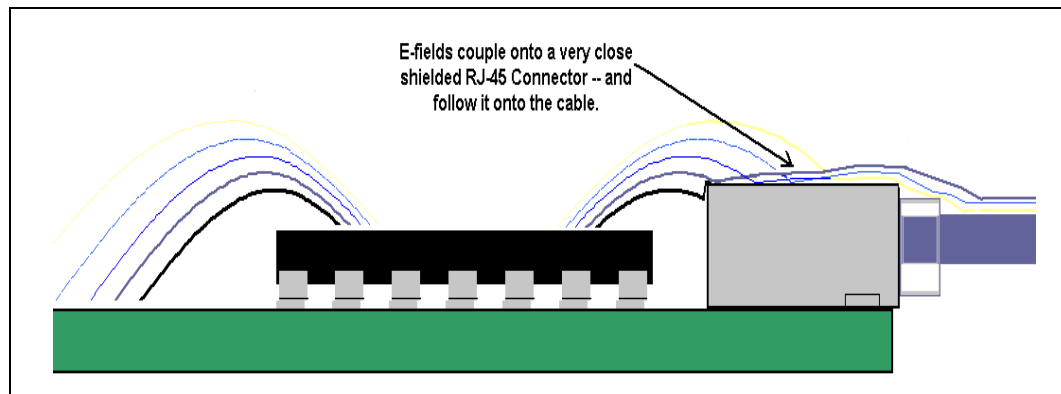
While it is generally a good idea to minimize lengths and distances, this figure also illustrates the need to keep the PHY away from the edge of the board and the magnetics module for best EMI performance.



**Figure 94. PLC Placement: At Least One Inch from I/O Backplane**



**Figure 95. Effect of LAN Device Placed Too Close To a RJ-45 Connector or Chassis Opening**





## 21.7 MDI Differential-Pair Trace Routing for LAN Design

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

## 21.8 Signal Trace Geometry

One of the key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the reference plane. To minimize trace inductance, high-speed signals and signal layers that are close to a reference or power plane should be as short and wide as practical. Ideally, the trace-width to trace-height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the neighboring planes.

Each pair of signals should have a differential impedance of  $100\ \Omega \pm 15\%$ .

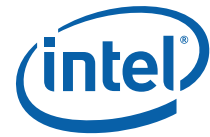
When performing a board layout, the automatic router feature of the CAD tool must not route the differential pairs without intervention. In most cases, the differential pairs will require manual routing.

*Note:* Measuring trace impedance for layout designs targeting  $100\ \Omega$  often results in lower actual impedance due to over-etching. Designers should verify actual trace impedance and adjust the layout accordingly. If the actual impedance is consistently low, a target of  $105\ \Omega$  to  $110\ \Omega$  should compensate for over-etching.

It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to  $10\ \Omega$ , when the traces within a pair are closer than 30 mils (edge-to-edge).

**Table 68. MDI Routing Summary**

Parameter	Main Route Guidelines	Breakout Guidelines <sup>1</sup>	Notes
Signal group	MDI_PLUS[0:3] MDI_MINUS[0:3]		
Microstrip/stripline uncoupled single-ended impedance specification	$50\ \Omega \pm 10\%$		
Microstrip/stripline uncoupled differential impedance specification	$100\ \Omega \pm 15\%$		2,3
Microstrip nominal trace width	Design dependent	Design dependent	4
Microstrip nominal trace space	Design dependent	Design dependent	3,5
Microstrip/stripline trace length	8 in (203 mm) maximum		6,7
Microstrip pair-to-pair space (edge-to-edge)	$\geq 7$ times the thickness of the thinnest adjacent dielectric layer		Figure 96
Stripline pair-to-pair space (edge-to-edge)	$\geq 6$ times the thickness of the thinnest adjacent dielectric layer		
Microstrip bus-to-bus spacing	$\geq 7$ times the thickness of the thinnest adjacent dielectric layer		
Stripline bus-to-bus spacing	$\geq 6$ times the thickness of the thinnest adjacent dielectric layer		

**Notes:**

1. Pair-to-pair spacing 3 times the dielectric thickness for a maximum distance of 500 mils from the pin.
2. Board designers should ideally target  $100\Omega \pm 15\%$ . If it's not feasible (due to board stack-up) it is recommended that board designers use a  $95\Omega \pm 10\%$  target differential impedance for MDI with the expectation that the center of the impedance is always targeted at  $95\Omega$ . The  $\pm 10\%$  tolerance is provided to allow for board manufacturing process variations and not lower target impedances. The minimum value of impedance cannot be lower than  $85\Omega$ .
3. Simulation shows  $80\Omega$  differential trace impedances degrade MDI return loss measurements by approximately 1 dB from that of  $90\Omega$ .
4. Stripline is NOT recommended due to thinner more resistive signal layers.
5. Use a minimum of 21 mil (0.533 mm) pair-to-pair spacing for board designs that use the CRB design stack-up. Using dielectrics that are thicker than the CRB stack-up might require larger pair-to-pair spacing.
6. For applications that require a longer MDI trace length of more than 8 inches (20.32 mm), it is recommended that thicker dielectric or lower Er materials be used. This permits higher differential trace impedance and wider, lower loss traces. Refer to Table 69 for examples of microstrip trace geometries for common circuit board materials.
7. If a LAN switch is not used, then the maximum trace length is 4 inches (102 mm). Mobile designs without LAN switch can range up to ~8 inches. Refer to Table 69 for trace length information.

**Table 69. Maximum Trace Lengths Based on Trace Geometry and Board Stack-Up**

Dielectric Thickness (mils)	Dielectric Constant (DK) at 1 MHz	Width / Space / Width (mils)	Pair-to-Pair Space (mils)	Nominal Impedance (Ohms)	Impedance Tolerance ( $\pm\%$ )	Maximum Trace Length (inches) <sup>1</sup>
2.7	4.05	4/10/4	19	$95^2$	$17^2$	3.5
2.7	4.05	4/10/4	19	$95^2$	$15^2$	4
2.7	4.05	4/10/4	19	95	10	5
3.3	4.1	4.2/9/4.2	23	$100^2$	$17^2$	4
3.3	4.1	4.2/9/4.2	23	100	15	4.6
3.3	4.1	4.2/9/4.2	23	100	10	6
4	4.2	5/9/5	28	$100^2$	$17^2$	4.5
4	4.2	5/9/5	28	100	15	5.3
4	4.2	5/9/5	28	100	10	7

**Notes:**

1. Longer MDI trace lengths may be achievable, but may make it more difficult to achieve IEEE conformance. Simulations have shown deviations are possible if traces are kept short. Longer traces are possible; use cost considerations and stack-up tolerance for differential pairs to determine length requirements.
2. Deviations from 100 $\Omega$  nominal and/or tolerances greater than 15% decrease the maximum length for IEEE conformance.

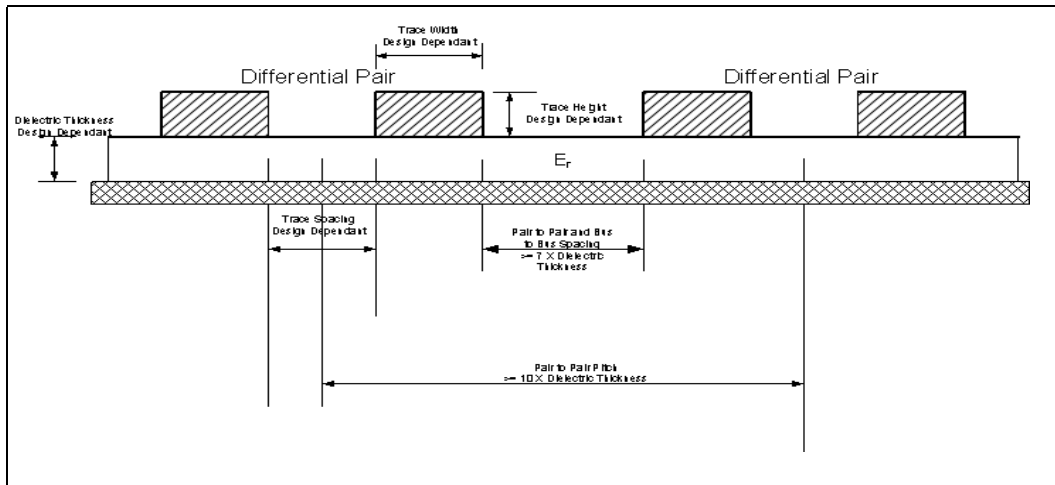
**Note:** Use the MDI Differential Trace Calculator to determine the maximum MDI trace length for your trace geometry and board stack-up. Contact your Intel representative for access.

The following factors can limit the maximum MDI differential trace lengths for IEEE conformance:

- Dielectric thickness
- Dielectric constant
- Nominal differential trace impedance
- Trace impedance tolerance
- Copper trace losses
- Additional devices, such as switches, in the MDI path may impact IEEE conformance

Board geometry should also be factored in when setting trace length.

Figure 96. MDI Trace Geometry





## 21.9 Trace Length and Symmetry

The differential traces should be equal in total length to within 10 mils (0.254 mm) per segment within each pair and as symmetrical as possible. Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. If a choice has to be made between matching lengths and fixing symmetry, more emphasis should be placed on fixing symmetry. Common mode noise can degrade the receive circuit's performance and contribute to radiated emissions.

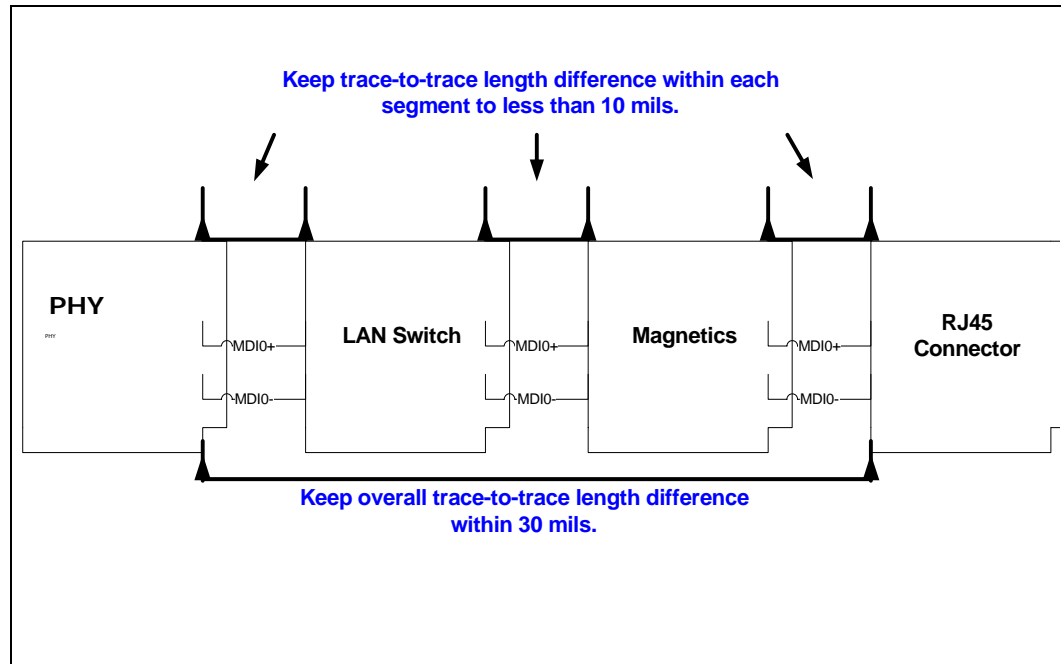
The intra-pair length matching on the pairs must be within 10 mils on a segment by segment basis. An MDI segment is defined as any trace within the same layer. For example, transitioning from one layer to another through a via is considered as two separate MDI segments.

The end to end total trace lengths within each differential pair must match as shown in the figure titled MDI Trace Geometry. The end to end trace length is defined as the total MDI length from one component to another regardless of layer transitions.

The pair to pair length matching is not as critical as the intra-pair length matching but it should be within 2 inches.

When using Microstrip, the MDI traces should be at least 7x the thinnest adjacent dielectric away from the edge of an adjacent reference plane. When using stripline, the MDI traces should be at least 6x the thinnest adjacent dielectric away from the edge of an adjacent reference plane.

**Figure 97. MDI Differential Trace Geometry**



**Note:** Similar topology applies to MDI routing from the SOC to the dock RJ45 connector.



## 21.10 Impedance Discontinuities

Impedance discontinuities cause unwanted signal reflections. Vias (signal through holes) and other transmission line irregularities should be minimized. If vias must be used, a reasonable budget is four or less per differential trace. Unused pads and stub traces should also be avoided.

## 21.11 Reducing Circuit Inductance

Traces should be routed over a continuous reference plane with no interruptions. If there are vacant areas on a reference or power plane, the signal conductors should not cross the vacant area. This causes impedance mismatches and associated radiated noise levels.

## 21.12 Signal Isolation

To maintain best signal integrity, keep digital signals far away from the analog traces. Also, keep the MDI traces away from the edge of an adjacent reference plane by a distance that is at least 7x the thickness of the thinnest adjacent dielectric layer (7x when using Microstrip; 6x when using stripline). If digital signals on other board layers cannot be separated by a ground plane, they should be routed perpendicular to the differential pairs. If there is another LAN controller on the board, the differential pairs from that circuit must be kept away.

Other rules to follow for signal isolation include:

- Separate and group signals by function on separate layers if possible. If possible, maintain at least a gap of 30 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, switching power supplies, or other similar devices.

## 21.13 Power and Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return. This will significantly reduce EMI radiation.

The following guidelines help reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions. Do not route over a split power or ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- All ground vias should be connected to every ground plane; and every power via, to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Split the ground plane beneath a magnetics module. The RJ-45 connector side of the transformer module should have chassis ground beneath it.



**Caution:** DO NOT do this, if the RJ-45 connector has integrated USB.

**Note:** All impedance-controlled signals should be routed in reference to a solid plane. If there are plane splits on a reference layer and the signal traces cross those splits then stitching capacitors should be used within 40 mils of where the crossing occurs. See [Figure 98](#).

If signals transition from one reference layer to another reference layer then stitching capacitors or connecting vias should be used based on the following:

If the transition is from power-referenced layer to a ground-referenced layer or from one voltage-power referenced layer to a different voltage-power referenced layer, then stitching capacitors should be used within 40 mils of the transition.

If the transition is from one ground-referenced layer to another ground-referenced layer or is from a power-referenced layer to the same net power-referenced layer, then connecting vias should be used within 40 mils of the transition.

**Figure 98. Trace Transitioning Layers and Crossing Plane Splits**

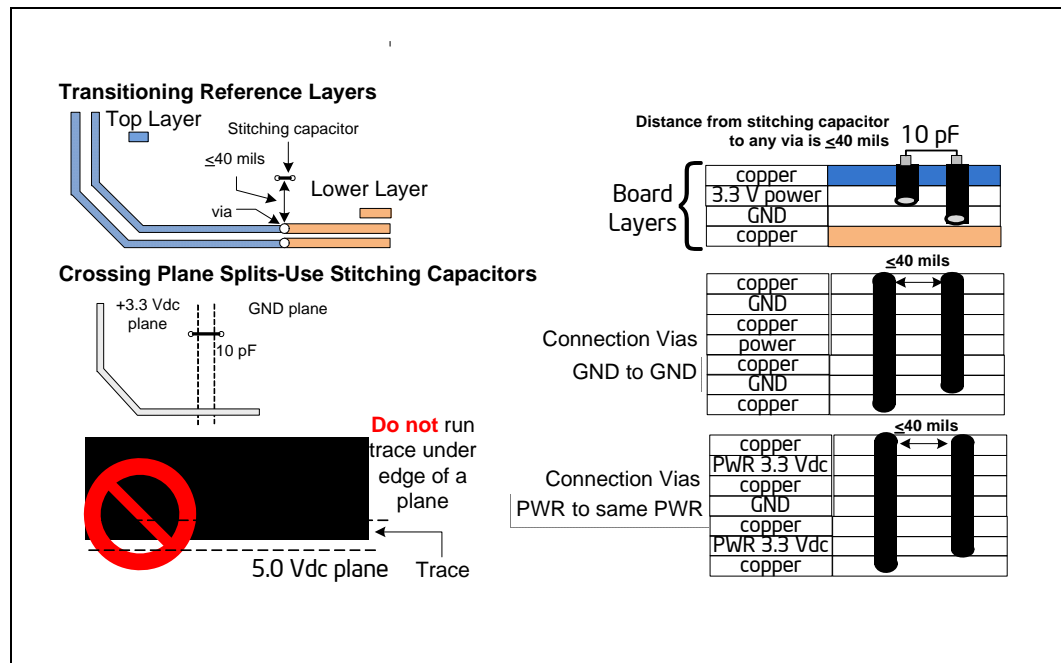


Figure 99. Via Connecting GND to GND

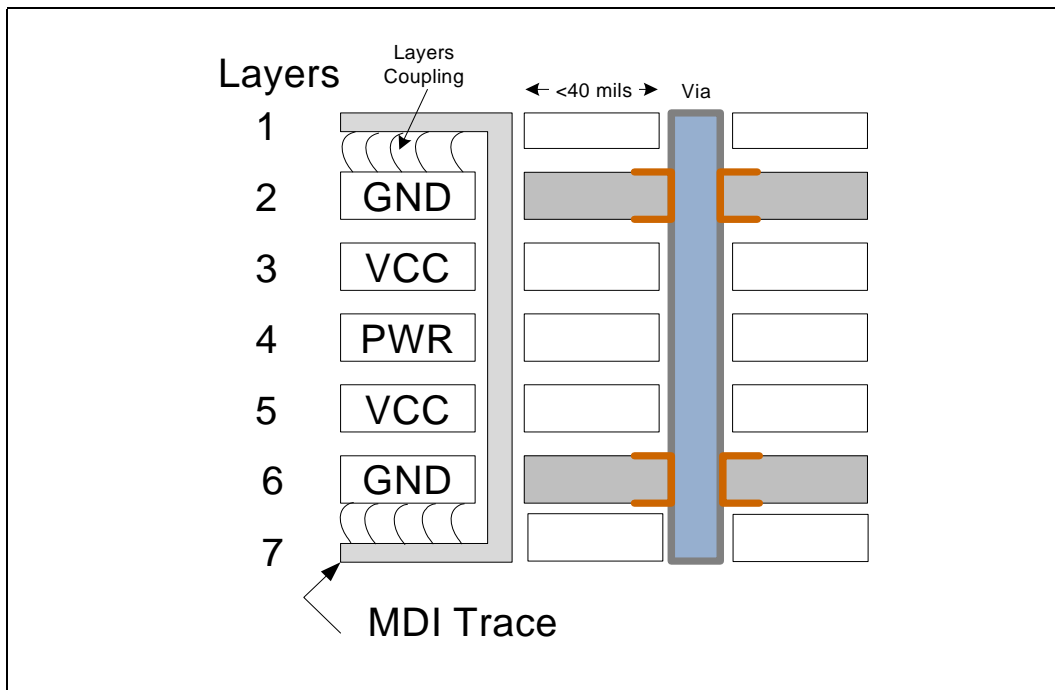
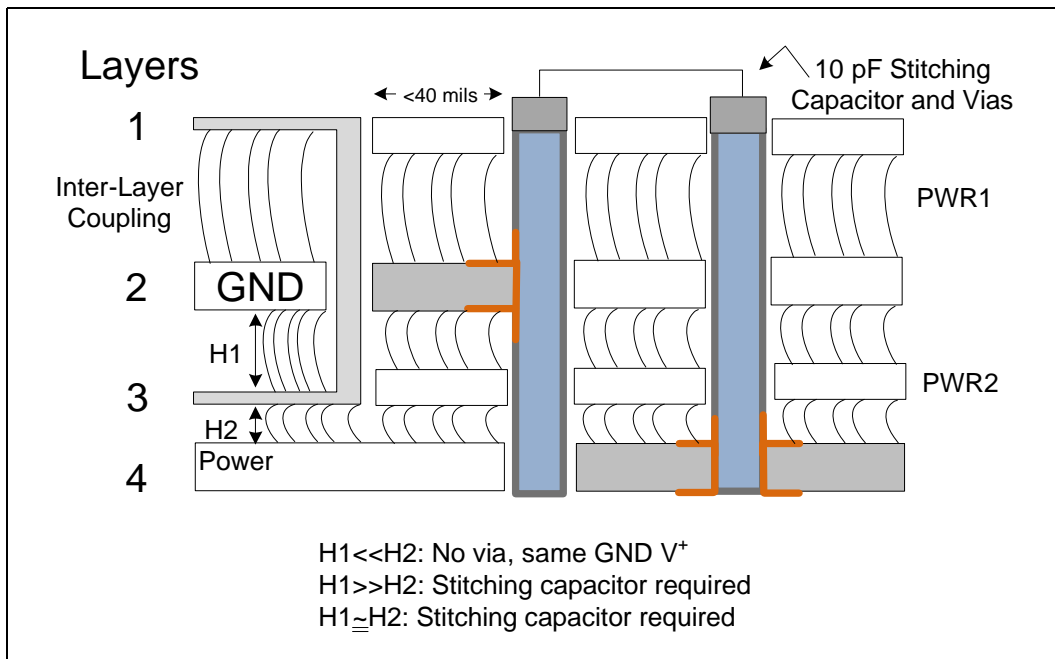


Figure 100. Stitching Capacitor between Vias Connecting GND to GND





## 21.14 Traces for Decoupling Capacitors

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and reduce the intended effect of decoupling capacitors. Also, for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Refer to the Power Delivery section for the PHY in regards to actual placement requirements of the capacitors.

## 21.15 Ground Planes under a Magnetics Module

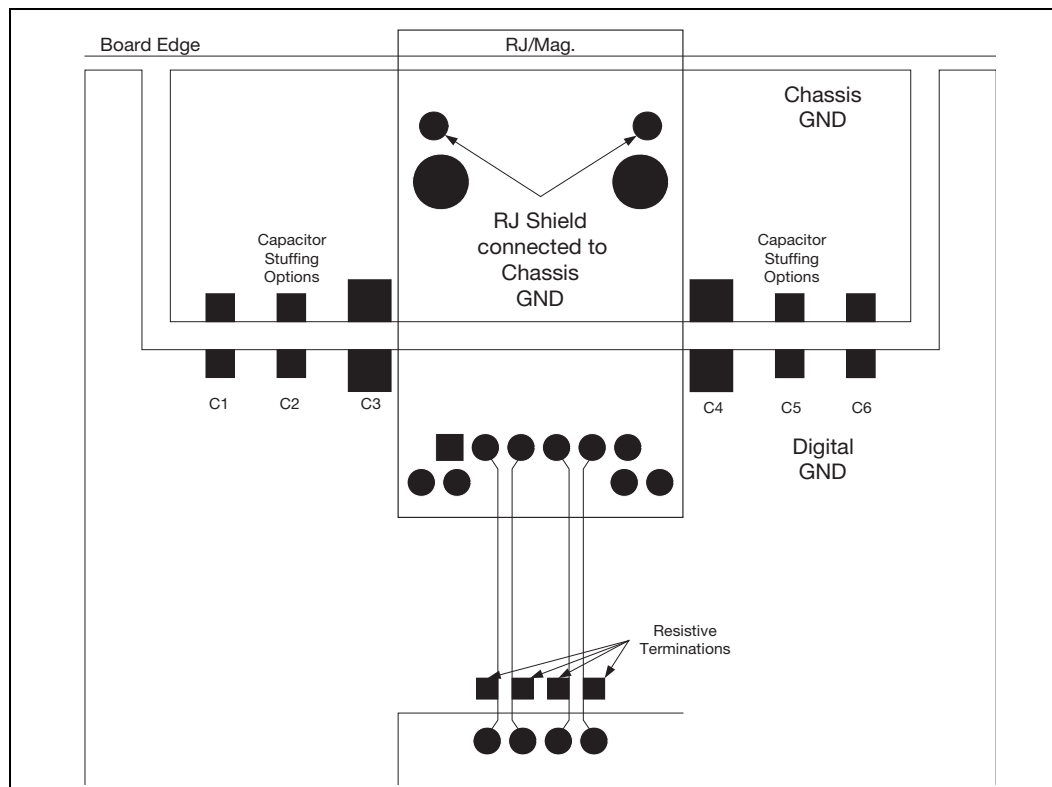
The magnetics module chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum. Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the magnetics. This arrangement also improves the common mode choke functionality of magnetics module.

**Caution:** DO NOT do this if the RJ-45 connector has integrated USB.

Figure 101 illustrates the split plane layout for a discrete magnetics module. Capacitors are used to interconnect chassis ground and signal ground.

Figure 101 shows the preferred method for implementing a ground split under an integrated magnetics module/RJ-45 connector.

Figure 101. Ideal Ground Split Implementation



**Table 70. Capacitor Stuffing Option Recommended Values**

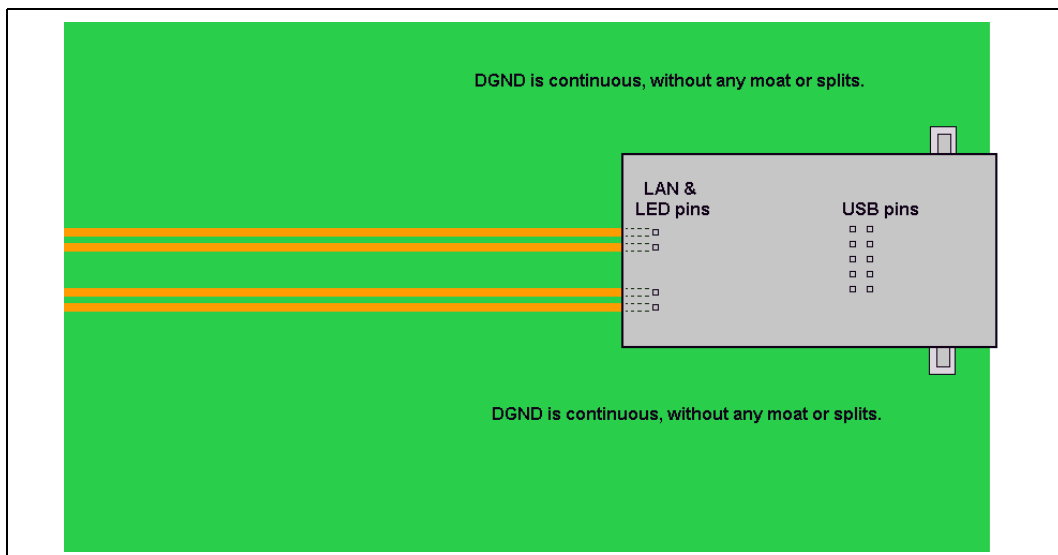
Capacitors	Value
C3, C4	4.7 $\mu$ F or 10 $\mu$ F
C1, C2, C5, C6	470 pF to 0.1 $\mu$ F

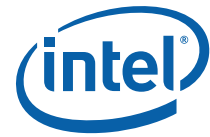
The placement of C1 through C6 may also differ for each board design (in other words, not all of the capacitors may need to be populated). Also, the capacitors may not be needed on both sides of the magnetics module.

*Note:* If using an integrated magnetics module without USB, provide a separate chassis ground “island” to ground around the RJ-45 connector. The split in the ground plane should be at least 20 mils wide.

Some integrated magnetics modules/RJ-45 connectors have recently incorporated the USB into the device. For this type of magnetics module, a chassis ground moat may not be feasible due to the digital ground required for the USB pins and their placement relative to the magnetics pins. Thus, a continuous digital ground without any moats or splits must be used. [Figure 102](#) provides an example of this.

**Figure 102. Ground Layout with USB**





## 21.16 Light Emitting Diodes

The device has three high-current outputs to directly drive LEDs for link, activity and speed indication. Since LEDs are likely to be integral to a magnetics module, take care to route the LED traces away from potential sources of EMI noise. In some cases, it may be desirable to attach filter capacitors.

LAN LED traces should be placed at least 6x (side by side separation) the dielectric height from sources of noise (ex: signaling traces) and susceptible signal traces (ex: reset signals) on the same or adjacent layers.

LAN LED traces should be placed at least 7x (broadside coupling) the dielectric height from sources of noise (ex: signaling traces) and susceptible signal traces (ex: reset signals) on the same or adjacent layers.

## 21.17 Considerations for Layout

The PHY MDI routing using microstrip requires a differential impedance of  $100 \Omega \pm 15\%$ . A 35 mils (0.889 mm) separation is required between pairs. The 35-mil separation can be reduced for 24 mils (0.61 mm) in breakout routing. All MDI traces must be referenced to ground.

## 21.18 Vibrational Mode

Crystals in the frequency range referenced above are available in both fundamental and third overtone. Unless there is a special need for third overtone, fundamental mode crystals should be used.

## 21.19 Nominal Frequency

The Ethernet controller uses a crystal frequency of 50.000 MHz. The 50 MHz input is used to generate a 125 MHz transmit clock for 100BASE-TX operation, and 10 MHz and 20 MHz transmit clocks, for 10BASE-T operation.

## 21.20 Frequency Tolerance

The frequency tolerance for an Ethernet Platform LAN Connect device is dictated by the IEEE 802.3 specification as  $\pm 50$  parts per million (ppm). This measurement is referenced to a standard temperature of 25 °C.

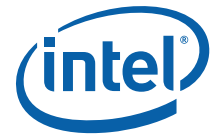
## 21.21 Troubleshooting Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LAN on Motherboard (LOM) designs.

1. Lack of symmetry between the two traces within a differential pair. Asymmetry can create common-mode noise and distort the waveforms. For each component and via that one trace encounters, the other trace should encounter the same component or a via at the same distance from the Ethernet silicon.
2. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
3. Excessive distance between the Ethernet silicon and the magnetics. Long traces on FR4 fiberglass epoxy substrate will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer than the four-inch guideline.



4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive EMI emissions and can cause poor transmit BER on long cables. At a minimum, for stripline other signals should be kept at least 6x the height of the thinnest adjacent dielectric layer. For microstrip it is 7x. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45 connector, and the Ethernet silicon.
5. Using a low-quality magnetics module.
6. Reusing an out-of-date physical layer schematic in a Ethernet silicon design. The terminations and decoupling can be different from one PHY to another.
7. Incorrect differential trace impedances. It is important to have about a 100- $\Omega$  impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling can lower the effective differential impedance by 5  $\Omega$  to 20  $\Omega$ . Short traces will have fewer problems if the differential impedance is slightly off target.



## 21.22 Power Delivery

In general planes should be used to deliver 3.3 Vdc and the Core voltage. Not using planes can cause resistive voltage drop and/or inductive voltage drop (due to transient or static currents). Some of the symptoms of these voltage drops can include higher EMI, radiated immunity, radiated emissions, IEEE conformance issues, and register corruption.

Decoupling capacitors (0.1 uF and smaller) should be placed within 250 mils of the LAN device. They also should be distributed around the PHY and some should be in close proximity to the power pins.

The bulk capacitors (1.0 uF or greater) should be placed within 1 inch if using a trace (50 mils wide or wider) or within 1.5 inches if using a plane.

## 21.23 Routing Guidelines

**Table 71.** MACO\_TXDATA<1:0>; MACO\_TXEN; MACO\_MDC; MACO\_MDIO

	Breakout			
PCB Routing Layer(s) Optional	4 Layer	4 Layer	4 Layer	4 Layer
Transmission Line Segment	L <sub>a</sub>	L <sub>b</sub>	L <sub>c</sub>	L <sub>d</sub>
Routing Layer (Microstrip / Stripline / Dual Stripline)	MS	MS	MS	MS
Characteristic Impedance (Single-ended)	50 Ω +/- 10%			
Trace Width (w)	4.2 mil	4.2 mil	4.2 mil	4.2 mil
Trace Spacing(S2): Between GPIO Signals	4.2 mil	10 mil	10 mil	4.2 mil
Trace Spacing(S3): Between GPIO and other signals	4.2 mil	10 mil	10 mil	4.2 mil
Trace Segment Length	0.5" max	0.1" - 0.8"	0.1" - 3.0"	0.5" max
<b>Note:</b> * Keep L <sub>a</sub> + L <sub>b</sub> as short as possible to give the best margin on the overshoot/undershoot violation.				

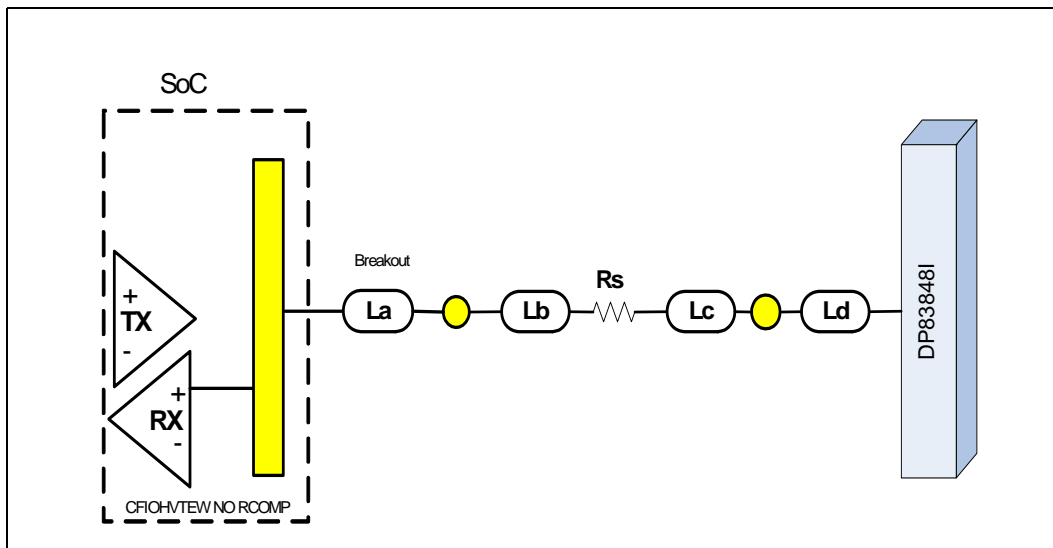
**Table 72.** MACO\_RXDATA<1:0>; MACO\_RXDV

	Breakout			
PCB Routing Layer(s) Optional	4 Layer	4 Layer	4 Layer	4 Layer
Transmission Line Segment	L <sub>a</sub>	L <sub>b</sub>	L <sub>c</sub>	L <sub>d</sub>
Routing Layer (Microstrip / Stripline / Dual Stripline)	MS	MS	MS	MS
Characteristic Impedance (Single-ended)	50 Ω +/- 10%			
Trace Width (w)	4.2 mil	4.2 mil	4.2 mil	4.2 mil

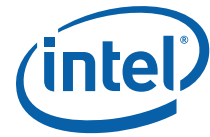
Table 72. MACO\_RXDATA<1:0>; MACO\_RXDV

	Breakout			
Trace Spacing(S2): Between GPIO Signals	4.2 mil	10 mil	10 mil	4.2 mil
Trace Spacing(S3): Between GPIO and other signals	4.2 mil	10 mil	10 mil	4.2 mil
Trace Segment Length	0.5" max	0.1" - 3.0"	0.1" - 0.8"	0.5" max
<b>Note:</b> * Keep Lc + Ld as short as possible to give the best margin on the overshoot/undershoot violation.				

Number of vias	max 2
Rs	33ohm +/- 5%
Reference Plane	Solid Ground Reference



§ §



## 22.0 Wireless Modules and Antenna Design Guidelines

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### 22.1 Introduction

There are a broad range of Wireless modules available suited to different regulatory, performance and user requirements. This chapter shall discuss choice of antenna materials, placement options and coexistence considerations for Intel® Quark SoC X1000-based designs.

Co-existence of multiple wireless modules and their antennas, among themselves and with the other systems and parts in the device can become a major problem if not considered in the initial stages of design.

SoC may support radios for:

- WiFi
- Bluetooth\* (BT)
- ZigBee (802.15.4)

### 22.2 WLAN System Integration Considerations

#### 22.2.1 Antenna Integration into the Platform

The goal of successful antenna integration on the system is four-fold:

1. Maintain good antenna efficiency for all antennas taken separately.
2. Ensure that platform noise coupling into each antenna is minimized (in-band noise).
3. Isolation between antennas is adequate to allow for:
  - a. Typical simultaneous radio usage scenarios to be supported (co-existence)
  - b. For radios supporting MIMO (multiple input and multiple output) or diversity, the spatial correlation and mutual coupling are low enough that maximum benefit can be derived from the additional radio chain

The following must be considered when deciding placement of antennas:

**Antenna size** – Larger sizes tend to provide better performance (gain, bandwidth, efficiency).

**Separation of radiation element from lossy structures including LCD enclosure:** Larger separation will provide higher bandwidth. In general, lower operational frequencies require larger separation compared to higher operational frequencies. Also, larger bandwidth considerations require larger separation from nearby metallic structures.

**Isolation between antenna ports:** Larger spatial separation is one way of increasing the isolation between ports of radio modules that operate in bands that are close to one another.



**Cable routing:** Cable routing that avoids regions of high noise and minimizes cable lengths allow for noise and losses to be minimized.

**Cable thickness (loss):** Thick cable (e.g., 1.37 mm) tends to be less lossy while being more expensive compared to thin cable (e.g., 1.13 mm). Double shielded cable is useful in ensuring that radio module sensitivity degradation is limited

**Antenna Orientation:** In some instances where the antennas have polarization discrimination, the relative orientation of the antennas can be used to enhance performance.

**Distance from Noisy components:** Impact of noisy components of the LCD, especially the timing controller chip in the display row-column drivers and un-shielded USB web cameras on the antenna must be considered. Modules must be shielded and antenna placement and cable routing must be optimized to minimize noise pickup by the antennas.

### 22.2.2 Antenna Coexistence

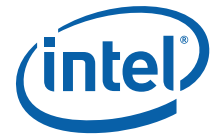
Radios Operating Simultaneously	Acceptable Performance Metric
WLAN interference to BT	While WLAN link is active, <i>BT voice</i> performance, as measured by Mean Opinion Score should not degrade below 3.5. Co-existence scheme between WLAN and BT should be enabled.
BT interference to WLAN	While BT link (Stereo audio) is active, care should be taken to ensure that the WLAN Radio is not de-sensed by more than acceptable levels. Contact WLAN module vendors for this information. (De-sense is measured through throughput vs. received power curves, with and without interference).
WLAN to ZigBee	When WLAN connection is active, ZigBee performance should not degrade from when ZigBee alone is active.
BT to ZigBee	When BT headset is being used with Stereo Audio, ZigBee performance should not degrade from when ZigBee alone is active.

### 22.2.3 WiFi Module

There is a broad offering of Intel and third-party WiFi modules supporting various 802.11 standards. Offerings are also differentiated by the number of inputs and outputs. In addition to cost, system integrators can keep in mind antenna placement options and wireless performance/quality requirements while making choices. MIMO-capable Wireless modules will provide additional flexibility in antenna placement in addition to providing better throughput. WiFi+BT integrated modules would be a good option for systems support Bluetooth as well, as these modules will ensure better co-existence and connectivity of both WLAN and Bluetooth. The current Intel® Quark SoC X1000 guideline is that the WiFi connectivity is provided via a daughter card/module.

The major design considerations for placement of a WiFi module on the platform are:

- Location of the module with respect to unintentional radiation sources on the platform (eg., DDR interface, platform clocks, and even emissions from peripherals)
- Placement of the module within an all-metal chassis without signal degradation
- Shielding of the module



#### 22.2.4 WiFi Module Connector Types

As WiFi modules are mounted on the platform, connectors plugging into them will add to the total z-height. OEM's can select connectors of low z-heights to keep the total z-height down. There are miniature coaxial RF connectors available in the market today with z-heights of the order of 2.5 mm to 1.4 mm.

#### 22.2.5 WiFi Antenna Placement

SoC systems are more likely to use metal enclosures for manufacturing reasons. In addition, antenna clearances will be much lesser than on conventional Thin and Light designs due to tighter z-height budgets. Both factors will create significant challenges in ensuring signal quality and reception comparable to a laptop with a plastic chassis and larger z-height budgets. System designers will have to strike a compromise between signal quality and cost while integrating antennas into the system.

The antenna should be placed as close to the module as possible to reduce losses in the board and/or cables, which can affect performance (throughput/range) directly. It is also important to ensure that the antenna is not covered by or in close proximity to the user's body and/or metallic body worn accessories. This is for two reasons; detuning of the antenna and high Specific Absorption Ratio (SAR) numbers. In addition the antenna should be kept away from noisy circuits and components such as the processor, memory, display (unshielded) etc. Minimum distances need to be maintained from metal parts depending on the type of antenna used.

The design must incorporate non conducting surfaces around the antenna for WiFi connectivity.

Maximizing the distance between the antenna and body to beyond the limit used for modular approval will allow for a reduction in test cases. This is best achieved by placing the antenna as close to the A-surface as possible.

Antenna performance is severely degraded if it is enclosed by metal or in close proximity to metal. Studies indicate that acceptable gains are possible with antenna separations of 5-mm to 10-mm from metal enclosures.

#### 22.2.6 Antenna Placement

When there is a metal surface surrounding the antenna, it is recommended to have plastic sections or insert molded plastic in the metal panel to maintain WiFi connectivity. Other options include cutouts and also placing antennas on the sides of the motherboard enclosure. In this case, care should be taken to ensure EMI from adjacent IO connectors does not interfere with the antenna reception.

The following placement options may be considered for closed lid operation:

1. **Base mounted WLAN antennas:** Incorporating 3G antennas in the same area will likely require additional components to achieve a compliant solution. Platform noise pickup from base mounted antennas needs to be measured before committing to a particular location as there is a higher risk of impact from platform noise with the use of base mounted antennas.
2. **Slot antennas cut into the chassis:** Slots can be cut into the surface of the antenna, near the apex of the lid and the cutout can be covered with plastic inserts. Such an antenna would be integrated into the chassis and special care must be given to the feeding mechanism, especially when materials not amenable to soldering such as aluminum are used. There are no discrete antennas with this solution. Multiple antenna SKUs will imply multiple chassis SKUs, so this option will need to be considered very early in the design cycle.



### 22.2.7 Antenna Cabling

The antenna cable is a lossy structure and hence needs to be as short as possible. Design choices can help reduce the cable length to the absolute minimum achievable. Studies have shown that acceptable performance metrics (loss/VSWR) can be achieved with 1.37mm diameter/double shielded cables.

### 22.2.8 Platform Noise Mitigation

Straddle mounted/Mid-mounted connectors help in reducing the EMI from the platform by reducing the lengths of connector pins which act as radiating elements. This is an additional benefit over and above the z-height saving that straddle-mounted connectors provide.

EMI sources on the platform (eg. right-angle connectors, large inductors etc.) will need to be identified by probing and may require to be shielded to cut down on EMI and improve antenna performance.

System designers must be aware of noise impact from several high speed digital interfaces there is the possibility of leakage from the connector.

### 22.2.9 Antenna Material Choices

- **FPC (Flex Printed Circuit):** This methodology has the advantage of printing antennas on flexible strips of film or plastic. The antennas will be extremely thin and can be accommodated easily into narrow spaces and can also be bent around corners. Prototyping and testing is also easier than other options. However care should be taken to ensure that the antenna is assembled in the exact same shape and orientation that it was validated in.
- **Stamped Metal:** Stamped metal antennas are low cost but will require an initial tooling cost, which may increase with the number of prototypes in the process of fine-tuning the antenna.
- **LDS (Laser Direct Structuring):** LDS is a process of antenna design and manufacturing that allows for low-cost, rapid prototyping. With the LDS technique the antenna can be etched onto almost any surface, thus providing many options for antenna integration.
- **Chip Antennas on high Dielectric material:** Another technique involves utilizing antennas built on high dielectric materials such as ceramic chip antennas. While the over the air coupling mechanism in such antennas is identical to antenna built with air core or low dielectric, the surface waves in the dielectric are tightly confined to the respective antennas providing enhancement in port to port antenna isolation. Chip antennas have the added benefit of smaller size, though there could be trade-offs associated with providing adequate keep out zones to maximize performance.

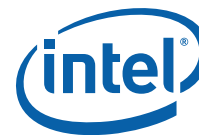
## 22.3 ZigBee System Integration Considerations

SoC based platforms supporting ZigBee (802.15.4)

### 22.3.1 ZigBee Antenna Placement

Similarly to module based WiFi solutions Zigbee solutions shall be based on daughter card/modules. The antenna placement guideline for such a module should be extracted from the relevant Zigbee device datasheet.

§ §



## Appendix A General Differential Signals Design Guidelines

### A.1 Introduction

The guidelines in this chapter are to improve routing for differential signals, such as Display, PCIe\*, USB, or SATA. The signal routing, via placement and bend optimization examples below apply to all high speed interfaces.

### A.2 General Differential Routing Guidelines

- **Do not** route traces under power connectors, other interface connectors, crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks. To minimize reflection, **Do not** place stubs, test points, test vias on the route. Utilize vias and connector pads as test points instead. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils.
- It can be helpful for testability to route the TX and RX pairs for a given port on the same layer and close to each other to help ensure that the pairs share similar signaling characteristics. If the groups of traces are similar, a measure of RX pair layout quality can be approximated by using the results from actively testing the TX pair's signal quality.
- Separate signal traces into similar categories, and route similar signal traces together (such as routing differential pairs together).
- Keep signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.

### A.3 General Differential Length Matching Guidelines

#### A.3.1 Length Matching and Length Formulas

Follow the specific interface length matching guidelines if provided. If not provided, use the below as a general guideline.

Table A-1. General Differential Pair Length Matching

Description	Units	Routing Recommendation
Within Layer Max Mismatch	mils	+/- 15
Total Length Max Mismatch	mils	+/- 10

The following are the length matching guidelines for differential-pairs:

- Each signal and its complement in a differential-pair should be length matched whenever possible on a layer-by-layer basis at the point of discontinuity. 'Within-layer' matching means that differential pairs should be matched within 15mils

before transitioning to a different layer. At any via transition the n/p mismatch for the entire route preceding the via cannot exceed 15mils.

- When trace length matching occurs, the matching should be made as close as possible to the point where the length variation occurs, as shown in [Figure A-1](#), so the discontinuity won't propagate across the channel. For example, length matching in a chipset breakout area or connector pin field should occur within the first 125 mils (3.175 mm) of the structure that causes the length mismatch.
- Serpentine layout introduces discontinuity to the channel and should be minimized so as to make it transparent to the signal. This is done by making its electrical length shorter than the signal rise time. In general, keeping serpentine routing length <100 mils is adequate. Trace spacing should not become greater than two times the original spacing. See [Figure A-2](#).
- In determining the overall length of a given signal in a differential-pair, use pad or pin edge-to-edge distances rather than the total etch present, unless the amount of trace routing inside each pad is identical. The amount of etch within a given pad is electrically part of the pad itself. In other words, only the etch outside of the pad edge is relevant to the overall length of a differential-pair. For example:
  - If the P signal of the differential-pair has an extra 5 mils (0.127 mm) of etch length compared to the N signal, and the extra 5 mils (0.127 mm) occurs due to extra etch extending into a component pad, the two signals should be considered identical length.
  - Similarly, trying to length match signals by adding etch inside a pad boundary (such as extra bends inside the pad itself) does not produce the intended length matching effect on the interconnection (see [Figure A-3](#)).

Figure A-1. Length Matching Example

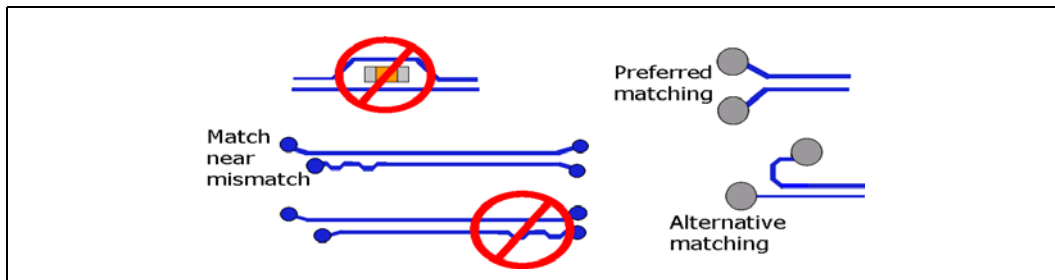


Figure A-2. Serpentine Example

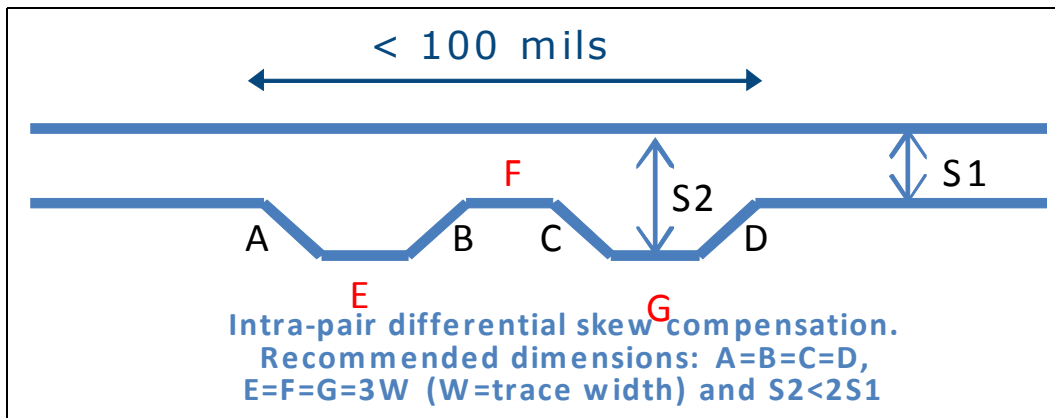




Figure A-3. Etch Located Within a Pad Example

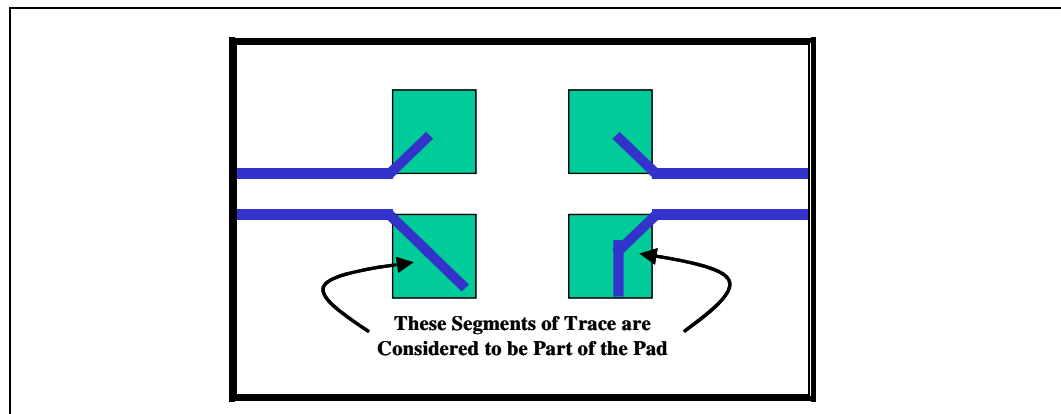


Figure A-4. Example of Good Length Matching

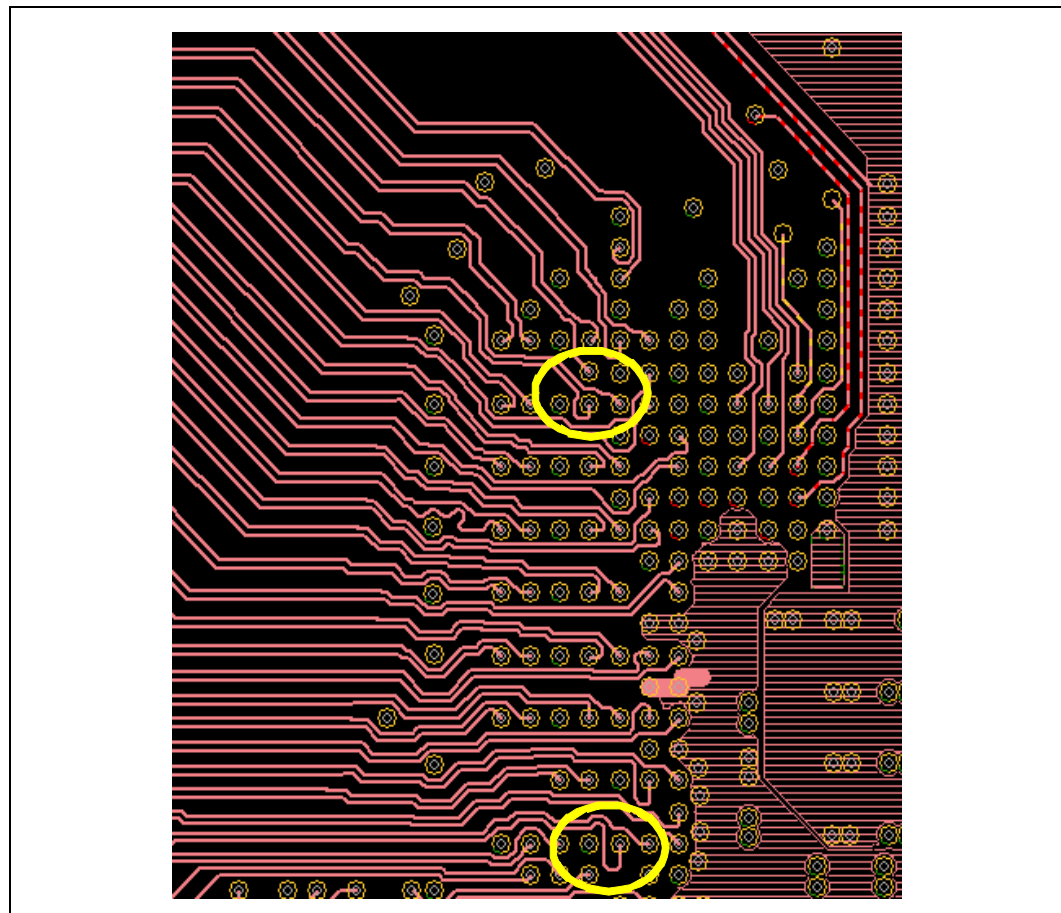
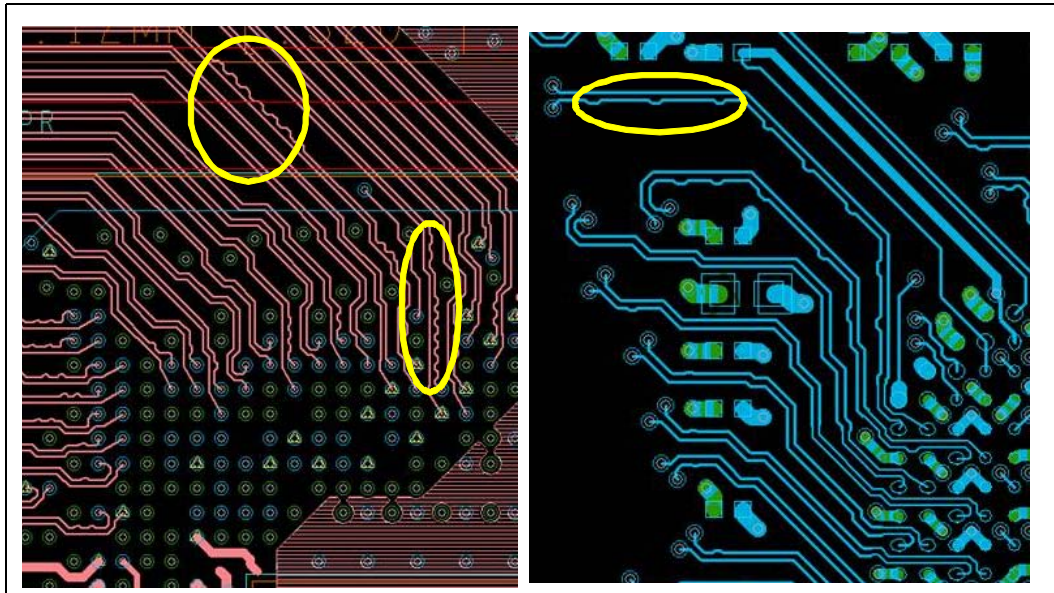


Figure A-5. Example of Poor Length Matching



## A.4 General Differential Stackup Guidelines

### A.4.1 Stackup and Layer Utilization Guidelines

#### A.4.1.1 General Dual-Stripline Support

In cases where high speed differential signals are routed in an 8- or 10- layers dual-stripline stack-up, please follow the guidelines in [Table A-2](#). [Figure A-6](#) illustrates the meaning of Tx-over-Tx, Rx-over-Rx, and Tx-over-Rx.

Table A-2. General Dual-Stripline Support

Tx -over-Rx Parallel Routing	Tx-over-Tx or Rx-over-Rx Parallel Routing	Tx-over-Rx or Tx-over-Tx or Rx-over-Rx Routing Orthogonal or with Angle
<ul style="list-style-type: none"> <li>Parallel routing not allowed</li> <li>Route with an offset of 15mil or greater as shown in <a href="#">Figure A-8</a>.</li> </ul>	<ul style="list-style-type: none"> <li>A maximum of 2 inches of parallel routing is allowed</li> </ul>	<ul style="list-style-type: none"> <li>Routing at an angle of at least 30 degrees significantly reduces layer-to-layer crosstalk. Route differential pairs at a 30, 45, 60, 90 etc degree angle. <a href="#">Figure A-7</a> shows orthogonal routing. <a href="#">Figure A-9</a> shows angled routing at less than 90 degrees.</li> <li>Allow maximum of 10 aggressor pairs to route over 1 DSL routing victim pair.</li> </ul>

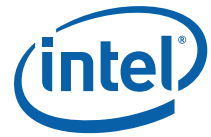


Figure A-6. Tx-over-Tx, Rx-over-Rx, and Tx-over-Rx

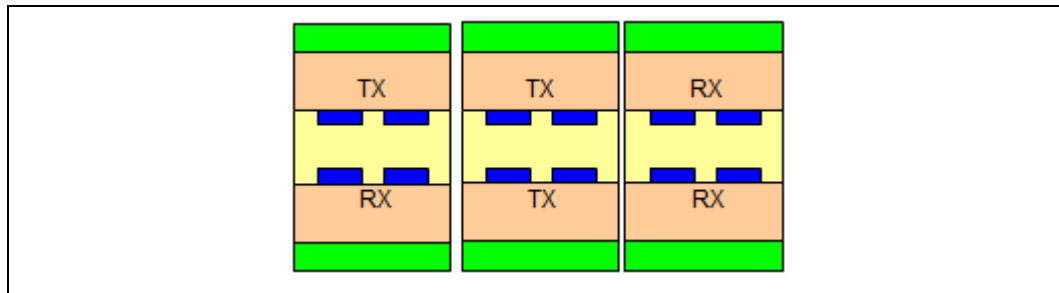


Figure A-7. Dual-Stripline Orthogonal Routing Recommendation

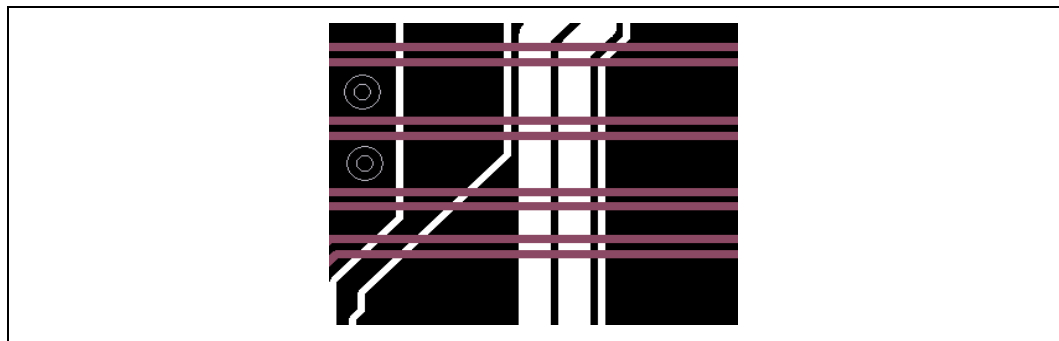


Figure A-8. Dual-Stripline High Speed Signal Dual Layer Routing Recommendation

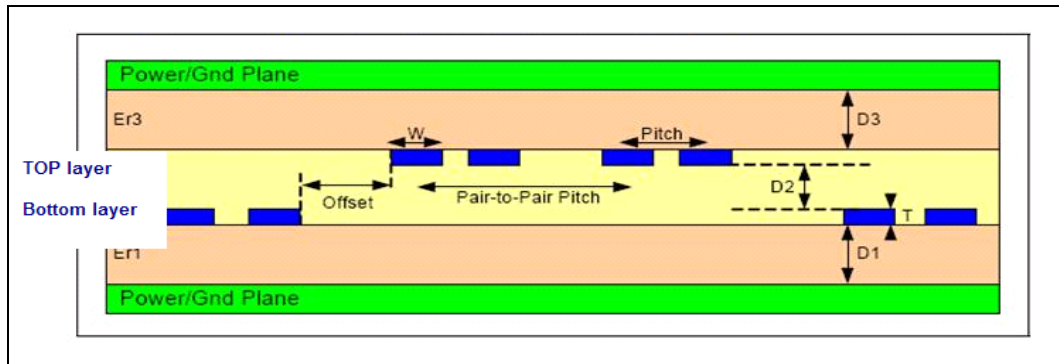
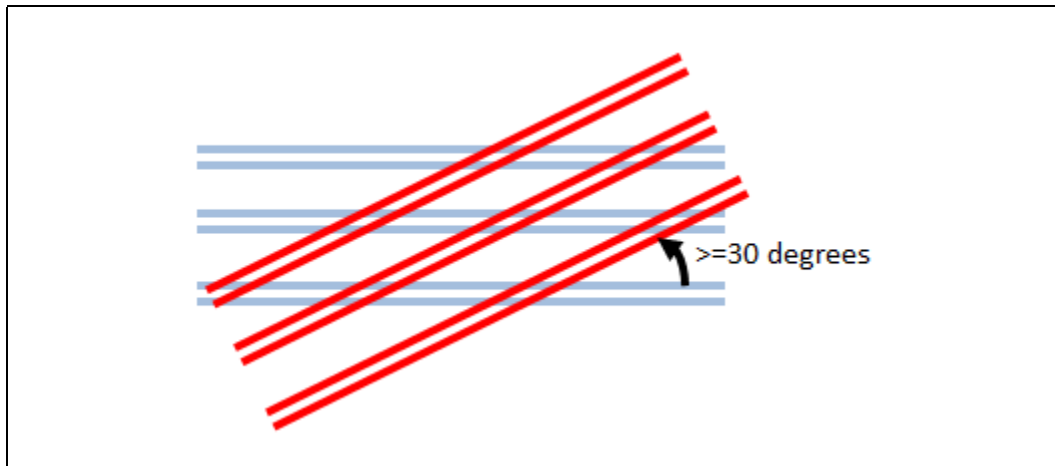


Figure A-9. Recommended Routing Angle to Reduce Layer-to-Layer Crosstalk

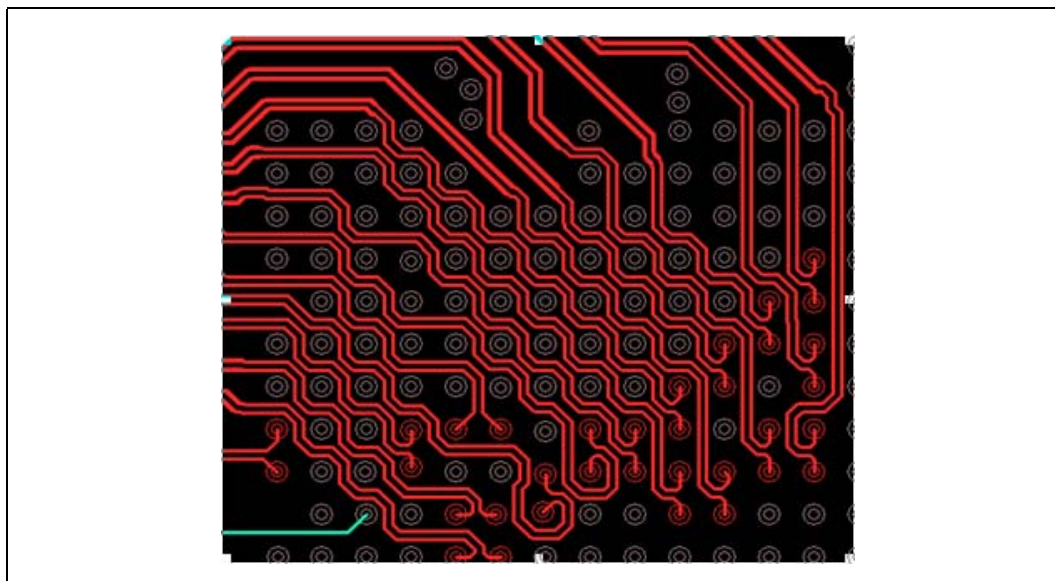


## A.5 General Differential Optimization Guidelines

### A.5.1 Breakout Example and Guidelines

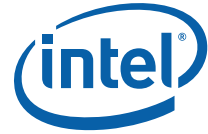
Maintain differential routing rules in package breakout areas.

Figure A-10. Mobile Package Breakout Example



Guidelines are as follows:

- **Differential-pair pitch** is measured from the center of each trace in the differential-pair. The distance from the center of either trace in a differential-pair to the same point of reference on an adjacent differential-pair is described as **interpair pitch (IPP)**. See [Figure A-11](#) for the illustration of differential-pair pitch and IPP.

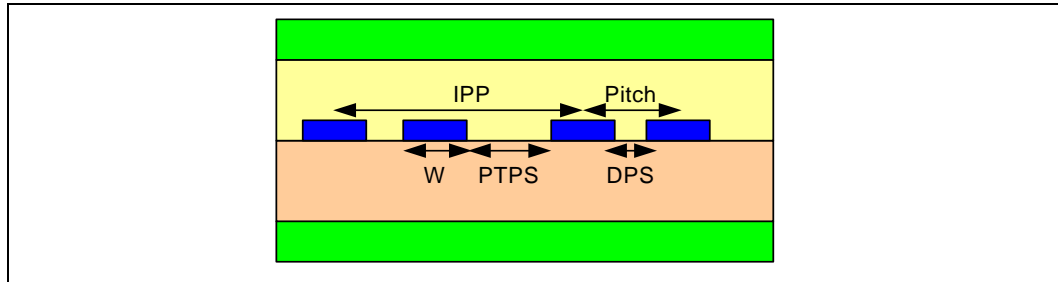


- **Differential-pair space** is measured from the edge of each trace in the differential-pair. The distance from the edge of one trace in a differential-pair to the near edge of an adjacent differential-pair is described as pair-to-pair space. See [Figure A-11](#) for the illustration of differential-pair space and pair-to-pair space.
- Maintain the best possible **lateral routing symmetry** between the two signals of a differential-pair. (See [Figure A-12](#)).
- Breakout routing geometries can be found in the Stackup and PCB Considerations section.
- The nominal trace width in the breakout region for processor and PCH can be decreased from 3.5 mils to 3 mils for stripline routing.

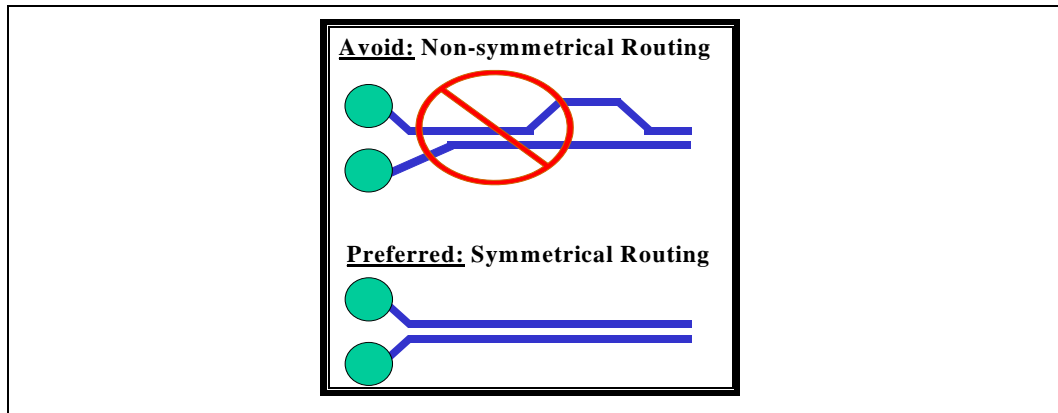
**Caution:** Maintain routing symmetry between the two signals of a differential-pair. Failure to maintain symmetry introduces an AC common mode voltage.

**Caution:** Reduced trace width will increase losses due to skin effects and reduced spacing will increase crosstalk. Therefore, it is recommended to keep breakout routing as short as possible.

**Figure A-11. Differential-Pair Spacing Diagram**



**Figure A-12. Symmetrical and Non-Symmetrical Routing Example**



### A.5.2 Via Placement and Via Usage Optimization

- Vias impact the overall loss and jitter budget. Route signals with a minimal number of vias.
- The via count can be reduced but not increased from the maximum interface via requirements given in this document.
- Remove pads from unused internal layers to minimize excess via capacitance.

- The differential-pair via placement must be symmetrical. Vias on the differential-pair should not only match in number but also in relative location.

Figure A-13. Via Pair Example

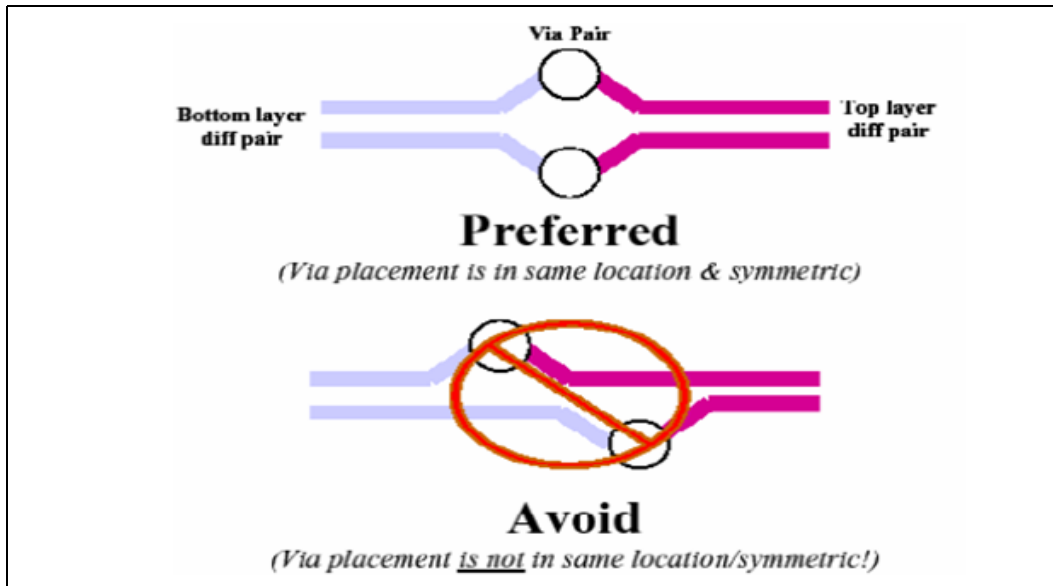
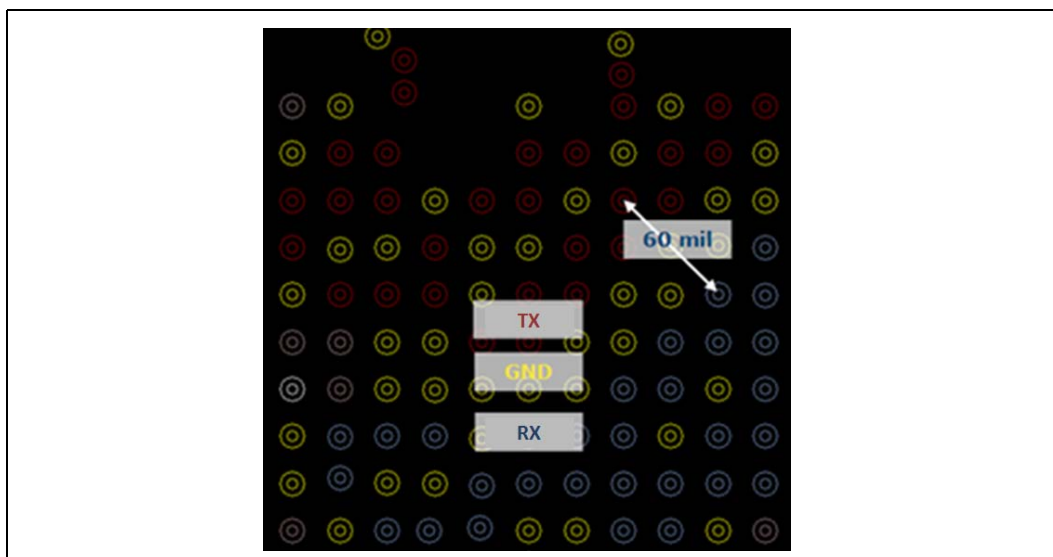


Figure A-14. Example - Via Placement 1



- The symmetric via pattern in [Figure A-15](#) below minimizes crosstalk between 2 differential pair, therefore the recommendation is to implement the pattern according to area availability.

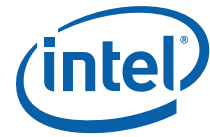
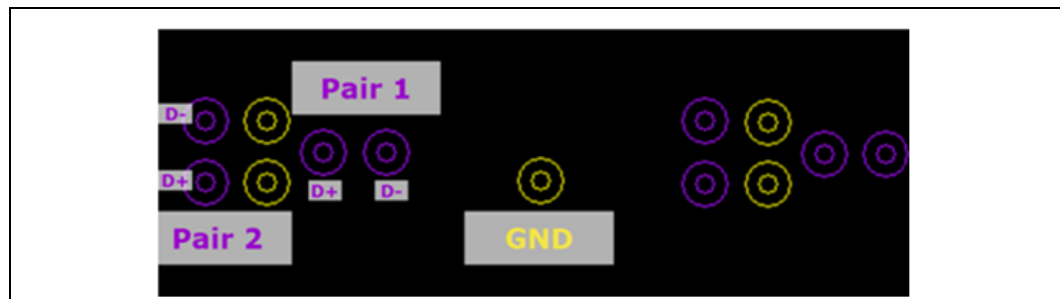
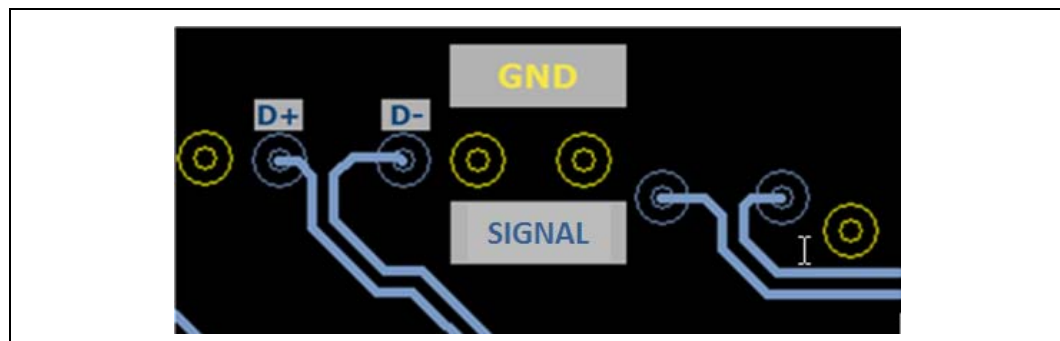


Figure A-15. Example - Via Placement 2



- For differential interfaces it is recommended 1:1 ratio of signal to GND via everywhere it is possible (Figure A-16).

Figure A-16. Package Breakout Example - Via Placement 3



### A.5.3 Bend Optimization Guidelines

Bends are a necessary component in routing differential signals. Guidelines for bends are as follows:

- Keep bends to a minimum. Bends can introduce common mode noise into the system, which can affect the signal integrity of the differential signal pair.
- If bends are required, they should be at a 135-degree angle or greater; there should be no 90-degree bends or turns. An adequate air gap should be maintained between the inside traces of a bend. The gap should be 4 times the trace width or greater. The lengths of the segments in a bend should be 1.5 times the trace width or greater. See Figure A-17 and Figure A-18 for examples.
- Match the number of left bends to the number of right bends to minimize skew due to length differences between each signal of the differential-pair.
- Alternate between left and right bends.

Matching the number of right and left turns and alternating bends helps to minimize the amount of skew between rising or falling edges, which minimizes the differential to common mode conversion.

Figure A-17. Acceptable Bends vs. Tight Bends Example

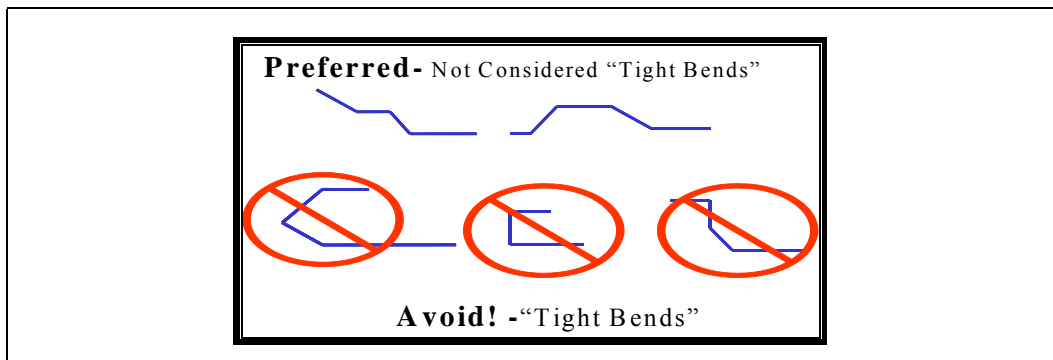
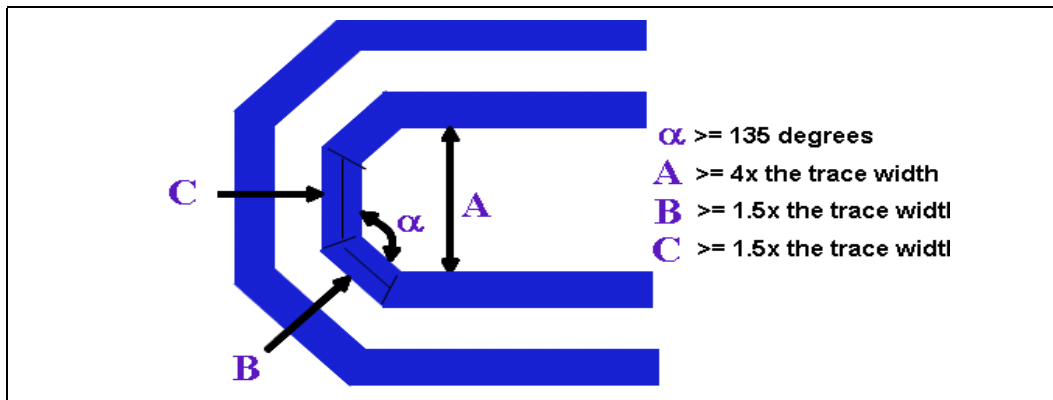


Figure A-18. Maximum Bend Angle



## A.6 General Differential Reference Planes Guidelines

Guidelines for reference planes are as follows:

*Note:*

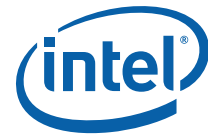
Even when routed as coupled differential-pairs, one trace can experience more coupling to its reference plane than to its routing pair.

- Traces should avoid discontinuities in the reference plane, such as splits and other voids.
  - A good plane reference helps to minimize any AC common mode voltage found on the differential-pair as well as benefiting signal quality and minimizing EMI.
- When routing near the edge of their reference plane, traces should maintain at least a 40-mil space keptout from the edge of the plane.

*Note:*

Referencing signals going over a board-to-board connector must be considered and stitching capacitors should be added at the connector as appropriate. For example, if a differential-pair is GND-referenced on the motherboard and the pair is  $V_{CC}$  referenced on the daughter card, then stitching capacitors must be added at the connector between  $V_{CC}$  and GND.

- One reference plane should be used for the entire length of the trace route.
  - In a traditional 8-layer stack-up, there are two microstrip/stripline routing channel pairs that each share a common reference layer. It is preferred that any layer transitions switch between these two layers, within this layer pair.



For example, Layer 1 and Layer 3 are tightly coupled to Layer 2 and form one layer pair; Layer 8 and Layer 6 are tightly coupled to Layer 7 and form another layer pair.

- If this cannot be accomplished, stitching vias must be used to tie the two planes together. The vias should be located within 200 mils and in symmetry with the two signal vias to minimize return path discontinuities.
- Differential signals should not cross any plane splits or voids. However, it may be necessary for a trace to be partially routed over a via anti-pad void in the chipset escape area. The amount of the trace that is over the void should be minimized in the length and percentage of the width of the trace. At worst, no more than half of the trace width should be over the via anti-pad at any given time.
  - If crossing a plane split is necessary, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1  $\mu$ F or lower in value) that bridge voltage plane splits close to where high-speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers.
  - As an example of bridging plane splits, a plane split that separates  $V_{5REF}$  and  $V_{CC3_3}$  planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to  $V_{5REF}$  and the other side should tie to  $V_{CC3_3}$ . Stitching caps provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

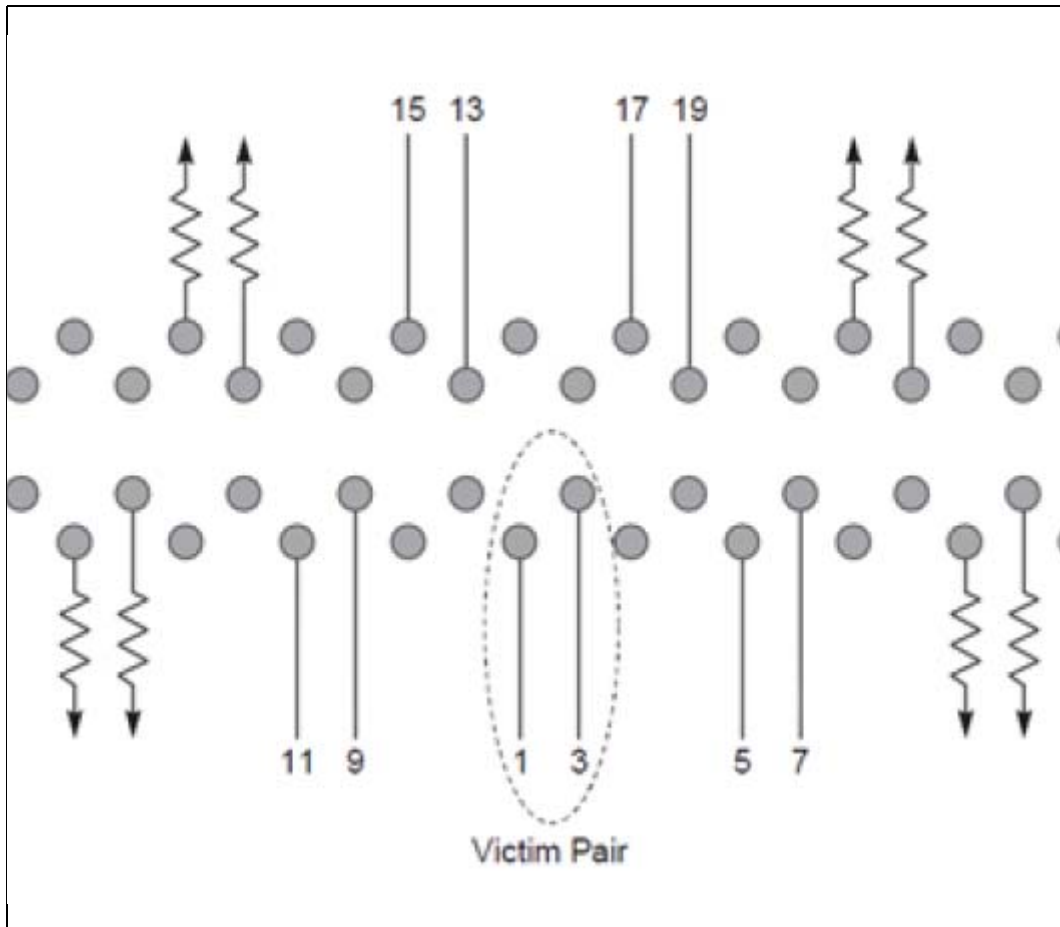
## A.7 General Docking Connector Recommendations for Differential Interfaces

Although various types and suppliers of docking connectors can be used, Intel recommends following the electrical characteristics in Table 5-3. This table lists the differential insertion loss, return loss, crosstalk, and impedance that Intel assumes when doing docking topology analysis for all differential interfaces. These are the specifications customers should check for when deciding a docking connector.

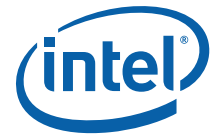
**Table A-3. Electrical characteristics for docking connector**

Parameter	Requirement	comment
Differential Insertion Loss (DDIL)	$\geq -1.2$ dB up to 3 GHz; $\geq -1.0$ dB up to 2.5 GHz; $\geq -0.035$ dB up to 240 MHz;	The measured differential S parameter shall be referenced to an 85 $\Omega$ differential impedance
Differential Return Loss (DDRL)	$\leq -12$ dB up to 3 GHz; $\leq -55$ dB up to 240 MHz;	The measured differential S parameter shall be referenced to an 85 $\Omega$ differential impedance
Differential (DDxtalk)	$\leq -30$ dB up to 3 GHz; $\leq -50$ dB up to 240 MHz;	This is a differential crosstalk requirement between a victim differential signal pair and all of its adjacent differential signal pairs at the same side of the connector as illustrated in Figure 5-19. The measured differential S parameter shall be referenced to an 85 $\Omega$ differential impedance.
Differential(oDDxtalk)	$\leq -40$ dB up to 3 GHz; $\leq -60$ dB up to 240 MHz;	This is a differential crosstalk requirement between a victim differential signal pair and all of its adjacent differential signal pairs from opposite sides of the connector as illustrated in Figure 5-19. The measured differential S parameter shall be referenced to an 85 $\Omega$ differential impedance.
TDR Target (DDZ) (Differential impedance)	80 -100 ohm	The connector shall be targeted for a 90 $\Omega$ differential impedance

Figure A-19. Example Port Assignment for Docking Connector



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## Appendix B Exposed Pad\* (e-Pad\*) Design and SMT Assembly Guide

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### B.1 Overview

This section provides general information about ePAD and SMT assemblies. Chip packages have exposed die pads on the bottom of each package to provide electrical interconnections with the printed circuit board. These ePADs also provide excellent thermal performance through efficient heat paths to the PCB.

Packages with ePADs are very popular due to their low cost. Note that this section only provides basic information and references in regards to the ePAD. It is recommended that each customer consult their Fab and assembly house to obtain more details on how to implement the ePAD package design. Each fab and assembly house might need to tune the land pattern/stencil and create a solution that best suits their methodology and process.

### B.2 PCB Design Requirements

In order to maximize both heat removal and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad or exposed heat slug of the package as shown in the following figures. Refer to the specific product datasheet for actual dimensions.

*Note:* Due to the package size, a via-in-pad configuration must be used Figure 101 and Figure 102 are general guidelines see Figure 103 for -specific via-in-pad thermal pattern recommendations.

Figure 103. Typical ePAD\* Land Pattern

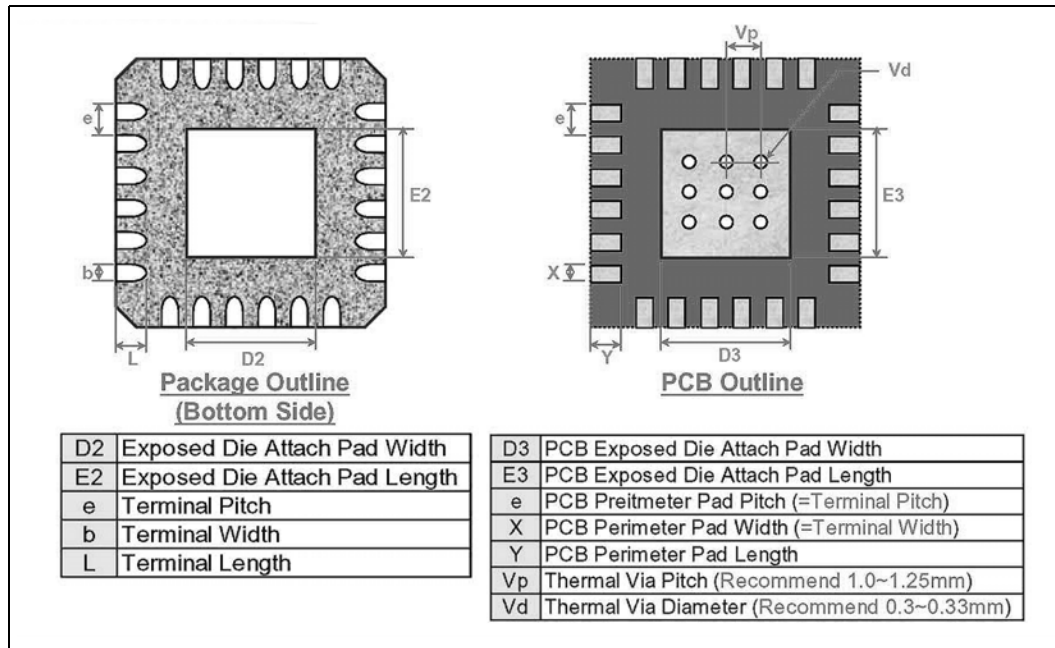
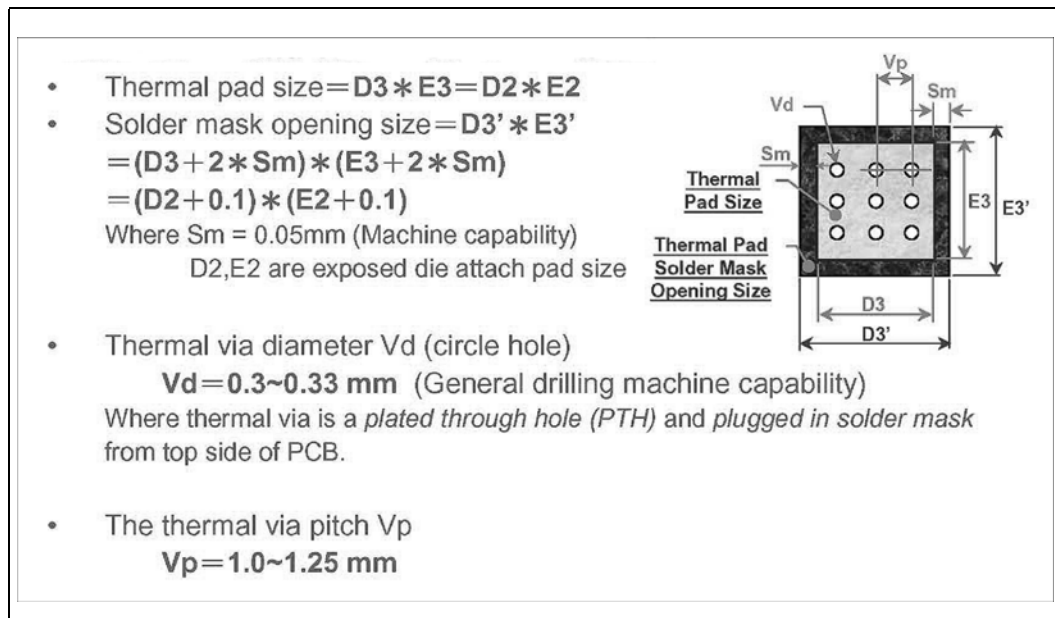


Figure 104. Typical Thermal Pad and Via Recommendations



Note: Encroached and uncapped via configurations have voids less than the maximum allowable void percentage. Uncapped via provides a path for trapped air to escape during the reflow soldering process.

Note: Secondary side solder bumps might be seen in an uncapped via design. This must be considered when placing components on the opposite side of the PHY.

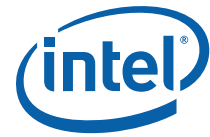
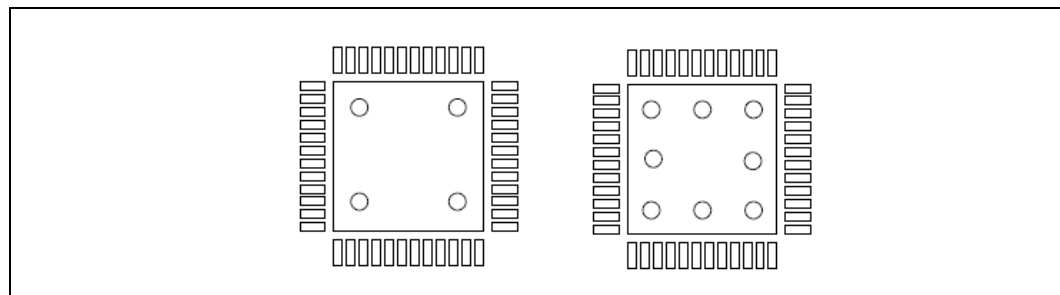


Figure 105. Recommended Thermal Via Patterns



### B.3 Board Mounting Guidelines

The following are general recommendations for mounting a QFN-48 device on the PCB. This should serve as the starting point in assembly process development and it is recommended that the process should be developed based on past experience in mounting standard, non-thermally/electrically enhanced packages.

### B.4 Stencil Design

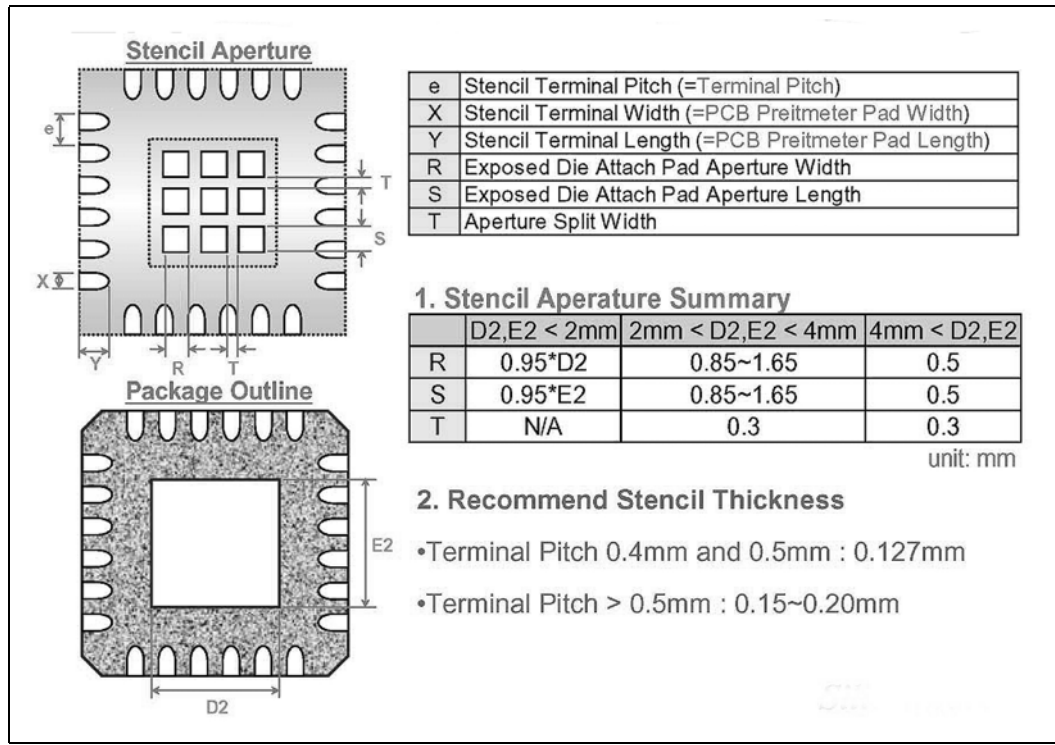
*Note:* For maximum thermal/electrical performance, it is required that the exposed pad/slug on the package be soldered to the land pattern on the PCB. This can be achieved by applying solder paste on both the pattern for lead attachment as well as on the land pattern for the exposed pad. While for standard (non-thermally/ -electrically enhanced) lead-frame based packages the stencil thickness depends on the lead pitch and package co-planarity, the package standoff must also be considered for the thermally/electrically enhanced packages to determine the stencil thickness. In this case, a stencil foil thickness in the range of 5 - 6 mils (or 0.127—0.152 mm) is recommended; likely or practically, a choice of either 5 mils or 6 mils. Tolerance wise, it should not be worse than  $\pm 0.5$  mil.

*Note:* Industry specialists typically use  $\pm 0.1$ -mil tolerance on stencil for its feasible precision.

The aperture openings should be the same as the solder mask openings on the land pattern. Since a large stencil opening may result in poor release, the aperture opening should be subdivided into an array of smaller openings, similar to the thermal land pattern shown in Figure 104.

*Note:* Refer to the specific product datasheet for actual dimensions.

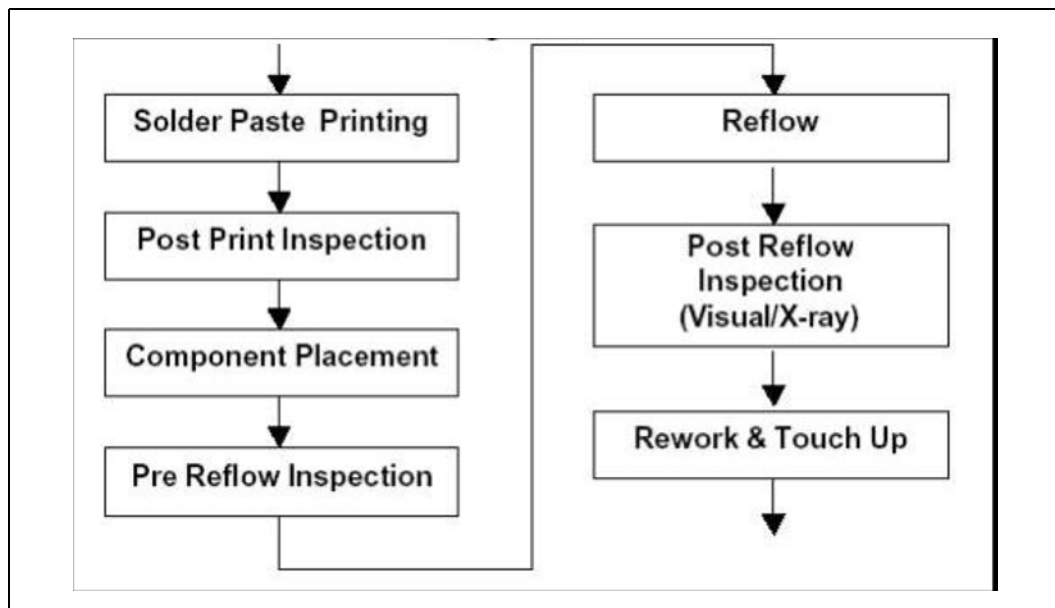
Figure 106. Stencil Design Recommendation



## B.5 Assembly Process Flow

Figure 105 shows the typical process flow for mounting packages to the PCB.

Figure 107. Assembly Flow

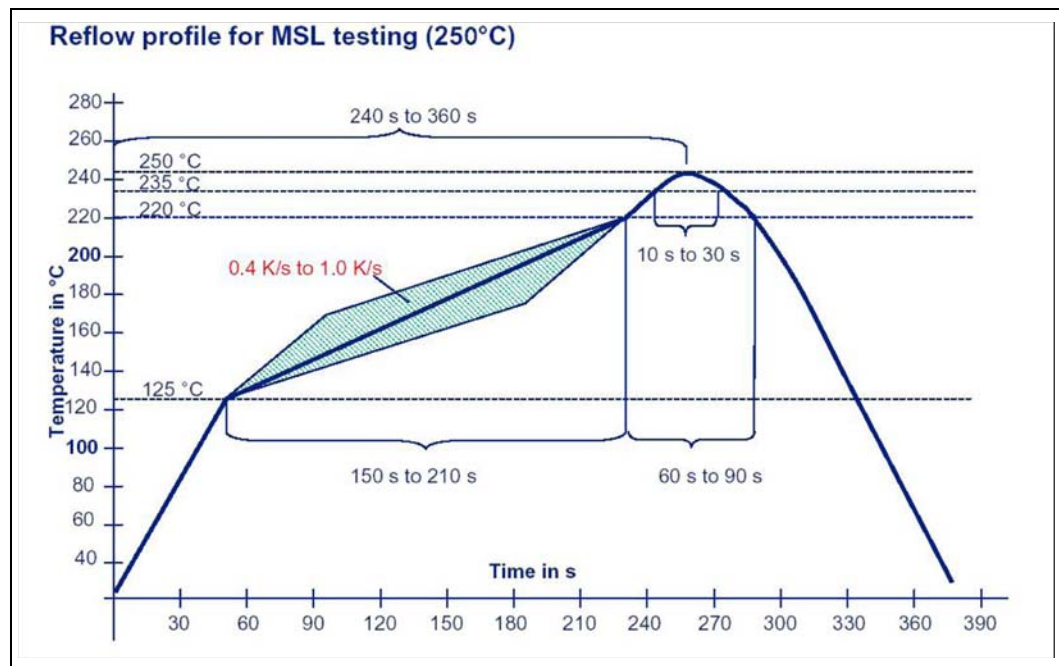




## B.6 Reflow Guidelines

The typical reflow profile consists of four sections. In the preheat section, the PCB assembly should be preheated at the rate of 1 to 2 °C/sec to start the solvent evaporation and to avoid thermal shock. The assembly should then be thermally soaked for 60 to 120 seconds to remove solder paste volatiles and for activation of flux. The reflow section of the profile, the time above liquidus should be between 45 to 60 seconds with a peak temperature in the range of 245 to 250 °C, and the duration at the peak should not exceed 30 seconds. Finally, the assembly should undergo cool down in the fourth section of the profile. A typical profile band is provided in Figure 106, in which 220 °C is referred to as an approximation of the liquidus point. The actual profile parameters depend upon the solder paste used and specific recommendations from the solder paste manufacturers should be followed.

Figure 108. Typical Profile Band



**Notes:**

1. Preheat: 125 °C - 220 °C, 150 - 210 s at 0.4 k/s to 1.0 k/s
2. Time at T > 220 °C: 60 - 90 s
3. Peak Temperature: 245-250 °C
4. Peak time: 10 - 30 s
5. Cooling rate: ≤ 6 k/s
6. Time from 25 °C to Peak: 240 - 360 s
7. Intel recommends a maximum solder void of 50% after reflow.

*Note:* Contact your Intel representative for any designs unable to meet the recommended guidance for E-pad implementation.

